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Development and Characterization of Three-Dimensional HZO Capacitor for Ultra-Dense Ferroelectric Non-Volatile Memories

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Dissertation Approval

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Declaration

I declare that, except where explicit reference is made to the contribution of others, this dissertation is substantially my own work and has not been submitted for any other degree at the Arab American University or any other institution.

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Dedication

To my family

Haifaa Kamil Mohamad Kmail

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This work was conducted at Interuniversity Center for Microelectronics and Nanotechnologies (CIME Nanotech) Laboratories at Grenoble through a collaboration between Arab American University - Palestine and Université Grenoble Alpes - France.

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Abstract

In this work, the ferroelectric behavior of the developed three dimensional hafnium zirconium oxide (HZO) capacitors are investigated. 300mm-integrated HZO metal ferroelectric metal (MFM) capacitors, with thicknesses ranging from 6nm to 10nm are deposited and fabricated by atomic layer and chemical vapor deposition (ALD and CVD) techniques. The electrical and structural properties are studied by exploring the influence of the main geometric and thermal parameters which include: aspect ratio, HZO thickness, and rapid thermal annealing (RTA) temperature.

The crystallographic structure of the devices is characterized using grazing incidence X-ray diffraction (GIXRD). The optimal incident angle is selected to be 7°. Improved crystallinity and increased peak intensity are observed with increasing annealing temperature and HZO thickness. In addition, the samples with higher aspect ratio show higher peak intensities compared to the samples with lower aspect ratio. The structural analysis of the measurements shows the formation of HZO orthorhombic phase, and the optimal temperature at which the orthorhombic phase is stabilized is found.

For studying the electrical properties, positive-up-negative-down (PUND) technique is employed to determine remanent polarization ($2P_r$) of the hysteresis loops of ferroelectric devices. Higher aspect ratio samples demonstrated higher values of $2P_r$ which also improves with both higher thickness and annealing temperature. Endurance testing further revealed that thinner films annealed at moderate temperatures exhibited higher electrical stability, with some samples preserving endurance beyond 10^9 switching cycles before breakdown.

These results highlight the significance of 3D structural design and the role of aspect ratio in enhancing ferroelectric behavior in HZO-based devices. The results also emphasize the need to carefully optimize both the thermal treatment and film thickness to achieve stable and high-performance ferroelectric capacitors.

Keywords: Ferroelectricity, HZO, Aspect ratio, PUND, Orthorhombic.

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List of Definitions of Abbreviations

Abbreviations	Title
AI	Artificial intelligence
SRAM	Static random access memory
DRAM	Dynamic random access memory
CMOS	Complementary metal–oxide semiconductor
PZT	Lead zirconate titanate
Zr	Zirconium
HfO_2	Hafnium oxide
AR	Aspect ratio
TiN	Titanium nitride
HZO	Hafnium zirconium oxide
MFM	Metal-ferroelectric-metal
ROM	Read-only memory
PROM	Programmable read-only memory
EPROM	Erasable programmable read-only memory
EEPROM	Electrically erasable programmable read-only memory
FRAM	Ferroelectric random access memories
1T-1C	1 transistor - 1 capacitor
PL	Plate line
P	polarization
F	Free energy
T_C	Curie temperature

P–E	Polarization-electric field
P_r	Remanent polarization
E_c	Coercive fields
P_s	Saturation polarization
$BaTiO_3$	Barium titanate
m	Monoclinic
o	Orthorhombic
c	Cubic
t	Tetragonal
FeFETs	Ferroelectric field effect transistors
FTJs	Ferroelectric tunnel junctions
ZrO_2	Zirconium oxide
Hf	Hafnium
C–V	Capacitance-voltage
$Pca2_1$	polar orthorhombic phase
ALD	Atomic layer deposition
PEALD	Plasma enhanced atomic layer deposition
FGA	Forming gas annealing
SEM	Scanning electron microscope
GIXRD	Grazing incident X-ray diffraction
PUND	Positive-up-negative-down
RTA	Rapid thermal annealing
SNAP	No-atmosphere processing deposition technique
P-V	Polarization–voltage
PECVD	Plasma enhanced chemical vapor deposition

MIM	Metal-insulator-metal
CVD	Chemical vapor deposition
W	Tungsten
PDA	Post-deposition annealing
$TiCl_4$	Titanium tetrachloride
NH_3	Ammonia
HCl	Hydrogen chloride
TEMAHf	Tetrakis (ethylmethylamino) hafnium
TEMAZr	Tetrakis (ethylmethylamino) zirconium
ICP-RIE	Inductively coupled plasma reactive ion etching
SF_6	Sulfur hexafluoride
US	Ultrasonic bath
HDRF	High density radical flux
XRD	X-ray diffraction
XRR	X-ray reflectometry
ω	Omega
SE_2	Secondary electron detector
DHM	Dynamic hysteresis measurements
PM	Polarization field measurements
FM	Fatigue measurements

Chapter One: Introduction

This chapter introduces the fundamental concepts underlying ferroelectric memory and the motivation for using hafnium oxide–based thin films in advanced data storage technologies. It begins with general introduction followed by overview of semiconductor memory types and the limitations of conventional volatile and perovskite-based non-volatile memories. The discussion then outlines the principles of ferroelectricity, switching behavior, and material degradation, followed by the structural analysis basis using Bragg's law. This background establishes the framework for studying the influence of geometry, HZO thickness, and annealing conditions on the performance of TiN/HZO/TiN capacitors.

1.1 General Introduction

In recent years, the rabid progress in artificial intelligence (AI), embedded systems and machine learning applications has led to increasing demand for high-performance and effective data storage solutions. Semiconductor memory devices in the form of static and dynamic Random Access Memory (RAM) control fast access data storage in computer systems. But they have a major obstacle; they lose all of their data when the power is removed (Yoo *et al*., 2023). However, substituting a thin film ferroelectric capacitor, which can be permanently polarized to store digital data promises semiconductor memories that store as much data as standard RAM and access data as fast as they do, but are non-volatile (Bondurant *et al*.,1989).

Non-volatile memory represents promising candidate for memory computing and embedded AI processors. The prospect use of ferroelectric-based nonvolatile random-memory (FRAM) for storing data was reported since 1980s (Bondurant *et al* .,1989). One class of memory devices based on ferroelectric is the capacitor-based ferroelectric memory (Park., 2018). Non-volatile FRAM was successfully incorporated into a complementary metal–oxide semiconductor (CMOS) environment (Onishi *et al*., 1994). However, poor compatibility with the advanced technology nodes of CMOS technology was an obstacle for early devices of ferroelectric-based RAM. Indeed, perovskites materials, particularly

the lead zirconate titanate (PZT), formed the basis of conventional ferroelectric memories. This presents major challenges related to high processing temperature, complicated crystal structure, and the difficulty of scaling down the thickness of the ferroelectric layer below 70 -100 nm (Kim& Lee, 2006). Further scaling is not possible due to the high physical thickness of the perovskite layer (typically ~70 nm) and the incompetence to produce three dimensional (3D) capacitors, as in dynamic RAM (Park, 2018). Owing to the limited memory array size of perovskite-based FRAM capacitors, their use was restricted to niche applications.

The discovery of ferroelectric hafnium oxide (HfO_2) in 2011 has changed the paradigm of ferroelectric memories due to its advantages over the conventional perovskite-structure ferroelectrics. Ferroelectric HfO_2 is ideally suitable for ferroelectric field effect transistors and capacitors due to its premium compatibility to silicon technology. Indeed, it was shown that Si-doped HfO_2 can exhibit strong remnant electric polarization thanks to a stabilized non-centrosymmetric orthorhombic crystalline phase. This response opened many perspectives toward the long desired integration of FRAM memory cells in CMOS technology (Böscke *et al* ., 2011). In addition, HfO_2 is widely used in CMOS technology as a gate oxide layer and can be readily integrated into metal insulator metal (MIM) stacks with thin or ultrathin HfO_2 layers.

In previous studies, many dopants were reported to induce ferroelectricity in HfO_2 films with typical thickness of 10 nm. It is widely admitted that material stabilization in non-centrosymmetric orthorhombic phase due to Si doping leads to ferroelectricity of HfO_2 (Materlik *et al*., 2015). Ferroelectric properties of HfO_2 doped with other doping impurities have been proven (Böscke *et al*., 2011). In 2017, the influence of nearly 40 dopants was investigated on the phase stability in bulk hafnia, it was reported that the lanthanide elements have the strongest effect on HfO_2 orthorhombic phase stabilization (Batra *et al*., 2017). Among these elements which were used to dope HfO_2 in addition to Si, is zirconium (Zr). Zirconium is a particularly effective dopant due to its similar ionic radius and lattice structure to Hafnium (Hf).

Hafnium zirconium oxide (HZO) has obtained particular interest due to its excellent ferroelectric properties and compatibility with advanced semiconductor fabrication. As a binary alloy of hafnium and zirconium oxides, HZO is considered as a lead-free candidate with exceptional ferroelectric properties next to the good pyroelectric and piezoelectric properties (Hashemi, 2022). In addition, it exhibits a strong tendency to stabilize the ferroelectric orthorhombic phase, which is important for achieving remanent polarization at ultrathin dimensions. HZO-based capacitors, particularly in TiN/HZO/TiN designs, have demonstrated high remanent polarization values (>20 $\mu C/cm^2$), excellent endurance (>10^9 cycles), and strong scalability (Liang et al., 2021). These attributes, combined with its suitability for 3D combination, make HZO a leading material for next-generation ferroelectric non-volatile memory.

Beyond material selection, the physical design of memory structure plays a fundamental role in the performance. In conventional 2D ferroelectric capacitor structures, scaling down the device size reduces the effective charge stored in the capacitor, which will make the memory read-out operation more difficult. This becomes particularly significant in advanced CMOS nodes below 20 nm, where the reduced area and charge can impair detection sensitivity. This scaling limitation can be avoided by using 3D Metal/HfO_2/Metal structures. These structures increase the surface area available for polarization without enlarging the device footprint. Within 3D geometries, the aspect ratio (AR) becomes a key parameter influencing electric field distribution, polarization behavior device performance (Grenouillet *et al*., 2023).

This dissertation highlights some physical investigations on the structural and electrical properties of 3D ferroelectric capacitors with TiN/HZO/TiN structure. The ferroelectric HZO layer with thicknesses ranging from 6 nm to 10 nm is positioned between two titanium nitride (TiN) electrodes. The bottom electrode is formed with a thickness of 10 nm, while the top electrode is deposited at 5 nm. The capacitor structures were deposited on etched SiO_2 layer with two different group of wafers, one with 300nm thick SiO_2, the other with 500nm thick SiO_2. The aim of this varying is to obtain different aspect ratio. The study examines the influence of the parameter: aspect ratio, HZO thickness, and annealing temperature on the resulting crystallographic and ferroelectric properties.

The phase formation and crystallinity is investigated using GIXRD, while electrical characterization is conducted using PUND method to evaluate remanent polarization and endurance performance. The following sections of this chapter introduce the theoretical background and fundamental principles of ferroelectricity. Chapter two provides an overview of recent studies relevant to HZO-based ferroelectrics. Chapter three details the experimental methodologies used in devices fabrication and characterization. Chapter four presents the structural and electrical results, with a particular focus on the effect of aspect ratio, HZO thickness and annealing conditions. Finally, Chapter five offers concluding remarks, summarizes the key findings of this work, and outlines potential directions for future research in 3D ferroelectric capacitor design.

1.2 Overview of Semiconductor Memories

Memory plays a fundamental role in modern electronic systems, enabling the temporary or permanent storage of information necessary for computation. Semiconductor memories are broadly categorized based on their ability to retain data when power is removed, as shown in the classification tree in Figure 1.1. These categories are: volatile memory and non-volatile memory.

Volatile memories lose its content upon power loss. They include static random access memory (SRAM) and dynamic random access memory (DRAM). Static random access memory retains data as long as power is supplied, using flip-flop circuits built from transistors. It offers fast access speeds but is expensive and occupies more chip area. Dynamic random access memory stores data using a transistor-capacitor pair for each bit, enabling higher density and lower cost but requiring periodic refreshing due to charge leakage from the capacitor (Jacob *et al*., 2010).

Non-volatile memories by contrast, retain data without continuous power. It include read-only memory (ROM) and its reprogrammable variants such as programmable-ROM (PROM), erasable programmable-ROM (EPROM), and flash memory. These memories maintain their contents without power and differ primarily in how and how often they can

be programmed and erased. Flash memory, a widely used electrically erasable programmable-ROM (EEPROM) variant, allows high-density storage and electrical erasing of large data blocks, though it suffers from limited write endurance and slower speeds (Sze & Ng, 2021).

The evolution of memory technologies has also led to hybrid forms that blur the traditional boundaries between volatile and non-volatile behavior. These include non-volatile RAMs that aim to combine the speed and access flexibility of RAM with the data retention of ROM (Chen, 2016). Figure 1.1 presents a simplified classification of semiconductor memory types.

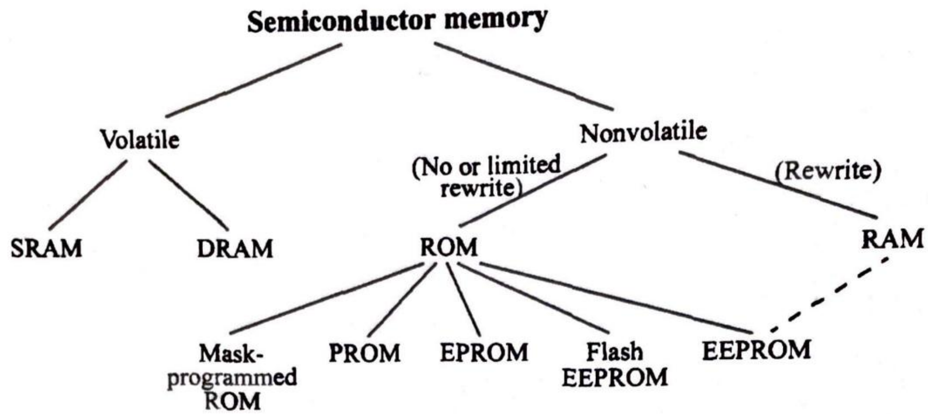

Figure 1.1: Classification of semiconductor memories (Sze & Mattis, 1970).

1.2.1 Ferroelectric Random Access Memories

A major goal in memory design is developing a memory that offers fast access, high endurance, non-volatility, and low energy consumption. One of the promising approaches is the use of ferroelectric materials that exhibit bistable polarization states. These materials can be electrically switched between two stable polarization directions, which represent binary states “0” and “1” (Mikolajick *et al*., 2020).

In this context, ferroelectric capacitors are used in memory cells to store digital information through reversible polarization. The remnant polarization, i.e. at zero voltage,

can be positive ($+P_r$) or negative ($-P_r$). If the two remnant polarization points at zero applied electric field are identified as "1" and "0", this bi-stable polarization allows the MFM structure to be used as binary memory (Scott, 2007). Hence, The read-out mechanism of a ferroelectric bit depends on the polarization state as depicted in Figure 1.2.

When the polarization state is already aligned with the applied voltage (bit "1"), the transient switching current is weak. In contrast, when the polarization is reversed during the read operation (bit "0"), a stronger switching current is generated. This switching current enables the detection of stored bits through their current signature, without destructive reading (Salvatore, 2011).

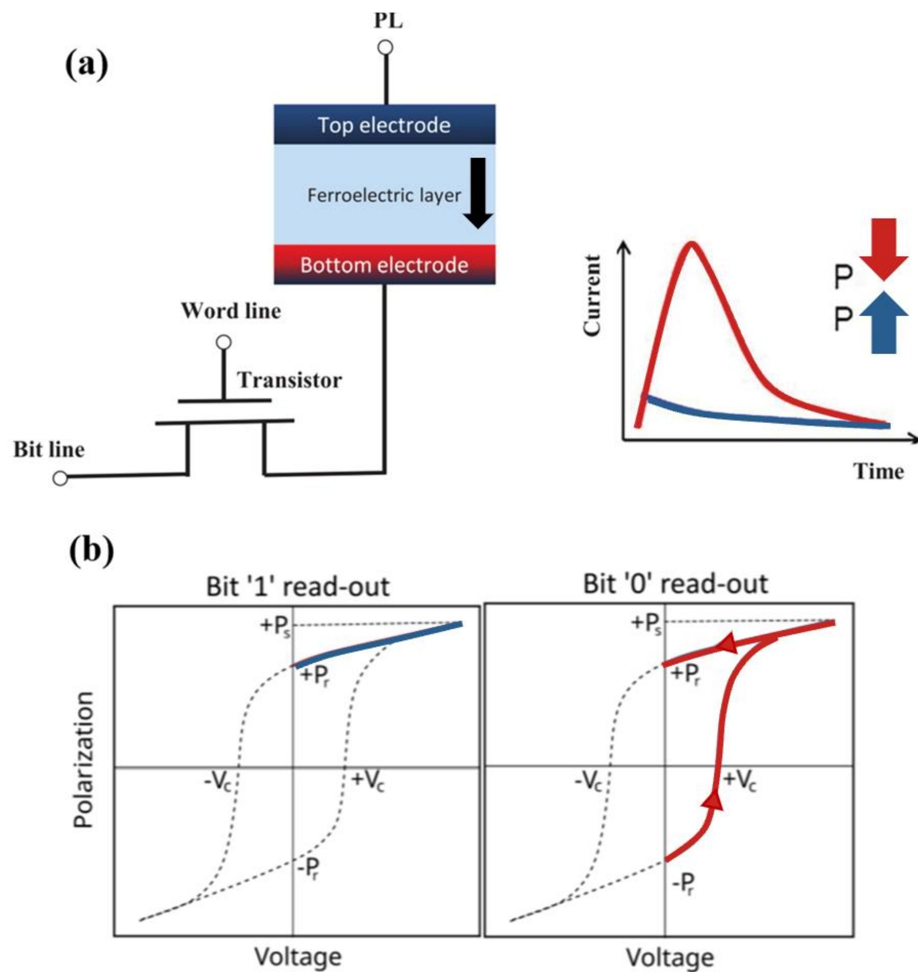

Figure 1.2: (a) Architecture of 1T-1C memory cell and current-response as a function of time for both polarization directions. (Banerjee *et al*., 2022). (b) Read out operation of FRAM, P-V Loop, adapted from Alrifai (2024).

This principle underlies the operation of FRAM, one of the key candidates for next-generation non-volatile memory technologies. It provides fast write/read operations. The architecture of a FRAM memory cell is similar to the one of a DRAM memory, except for the use of the ferroelectric material, instead of a dielectric to achieve the non-volatility. In a FRAM cell, the storage ferroelectric capacitor is connected in series to a transistor in 1 Transistor - 1 Capacitor (1T-1C) architecture as represented in Figure 1.2 (a).

During the write operation of a “1” or “0”, the word line is pulsed to enable the access to the storage capacitor, while during read operation, a voltage is applied to the plate line (PL) and the word line is simultaneously pulsed. Since the read operation is destructive, a further rewriting step is required to bring back the memory cell in the initial state (Segantini, 2023).

1.3 Fundamentals of Ferroelectricity

In materials science, understanding how materials respond to electric fields has led to the discovery of classes of materials with unique polarization behaviors. Most conventional dielectric materials exhibit a linear relationship between polarization and electric field, where the induced polarization vanishes once the external field is removed. However, a distinct class of materials known as ferroelectrics demonstrates a fundamentally different response. These materials possess a spontaneous electric polarization that can be reversed by the application of an external electric field, enabling two stable polarization states (Dawber *et al*., 2005).

This bistability arises from the non-centrosymmetric crystal structures of ferroelectric materials, which allows internal electric dipoles to align in preferred orientations under external stimuli. Unlike ordinary dielectrics, the polarization in ferroelectrics does not linearly follow the applied field but instead traces a hysteresis loop. This hysteretic behavior, is a hallmark of ferroelectric switching and forms the basis for their application in non-volatile memory technologies (Mikolajick *et al*., 2020). Figure 1.3 shows this difference between the dielectric and ferroelectric materials.

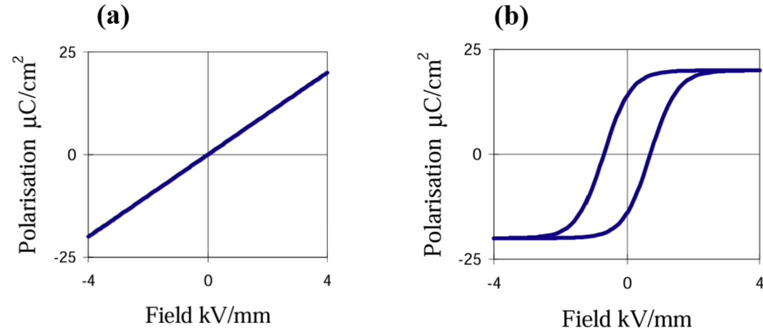

Figure 1.3: Polarization vs. electric field response in (a) dielectric and (b) ferroelectric materials (Stewart *et al*., 1999).

1.3.1 Classification of Polar Dielectrics

The ability of a material to exhibit ferroelectricity is governed by its crystallographic symmetry. Out of the 32 crystal point groups in solid-state physics, only 21 are non-centrosymmetric, meaning they lack a center of inversion. This absence of symmetry allows for a net dipole moment to exist within the crystal unit cell, enabling certain materials to develop polarization responses under external field (Lines & Glass, 2001; Dawber *et al*., 2005).

Among these 21 non-centrosymmetric point groups, 20 exhibit piezoelectricity, a property where mechanical stress induces electric polarization. A subset of 10 point groups are pyroelectric, meaning they possess a permanent spontaneous polarization that varies with temperature. Pyroelectrics maintain this polarization even in the absence of an applied electric field, distinguishing them from general piezoelectric.

However, not all pyroelectric materials are capable of reversing their polarization under an external field. Only those that can switch their spontaneous polarization direction qualify as ferroelectric (Li *et al*., 2022). This hierarchical relationship is depicted in Figure 1.4, where ferroelectrics appear as a specialized subset within the broader categories of pyroelectrics and piezoelectrics. Importantly, all ferroelectric materials are inherently pyroelectric and piezoelectric, but the reverse does not hold true.

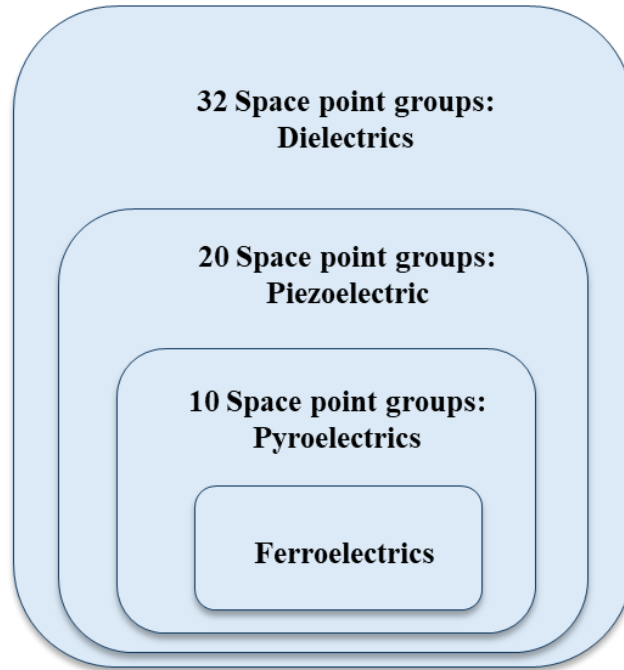

Figure 1.4: Schematic diagram of the dielectrics classification.

The fundamental distinction between ferroelectric and non-ferroelectric materials lies in inversion symmetry. Centrosymmetric crystals those with a center of symmetry exhibit spatial configurations such that each atomic position at (x, y, z) has a corresponding one at (−x, −y, −z). This symmetry ensures that any intrinsic dipole moment is cancel out, giving materials. In contrast, non-centrosymmetric crystals lack this inversion point, enabling the formation of a net dipole moment and, in specific structures, spontaneous and reversible polarization (Gorfman & Zhang, 2024).

It is this crystallographic asymmetry, combined with the material's polar axis and bonding environment, that makes ferroelectricity possible. Changes in external conditions mechanical, electrical, or thermal can influence atomic displacements within the unit cell, thereby modulating the material’s polarization state. Therefore, ferroelectric materials must not only be non-centrosymmetric, but also possess a polar lattice configuration capable of supporting domain switching.

1.3.2 Electric Polarization and Ferroelectricity

When a dielectric is subjected to an external electric field E, its charges are displaced and acquire an average dipole moment. The macroscopic polarization vector **P** is defined as the dipole moment per unit volume (Jackson, 1998):

$$\mathbf{P} = \frac{\mathrm{dN}\langle \mathbf{p} \rangle}{\mathrm{dV}} \tag{1.1}$$

where N is the number of dipoles per volume $V$and $\langle \mathbf{p} \rangle$ their average dipole moment. Two main contributions to polarization are usually distinguished; the first one is deformation (electronic) polarization which arising from the displacement of the electron cloud with respect to the nucleus under E. The induced dipole is proportional to the field:

$$\mathbf{p} = \alpha_d \mathbf{E} \tag{1.2}$$

Where α_d is the electronic polarizability. The second contribution is orientational polarization, typical of polyatomic molecules with permanent dipoles. In zero field, these dipoles are randomly oriented, but under E, they tend to align, yielding a mean dipole moment (Jackson, 1998):

$$\langle \mathbf{p} \rangle = \alpha_0 \mathbf{E}, \quad \alpha_0 = \frac{p_0^2}{3k_B T} \tag{1.3}$$

Where p_0 is intrinsic dipole moment, k_B is the Boltzmann constant and T is the temperature. At high fields, saturation occurs as all dipoles align with the field. The ferroelectric dielectric, additionally exhibit a spontaneous polarization P_s even in the absence of external field. Their polarization can be written as (Lines & Glass, 2001):

$$P = \varepsilon_0 \chi E + P_s \tag{1.4}$$

Where ε_0 is the vacuum dielectric constant and χ is the dielectric susceptibility.

In these materials, the P–E relation is hysteretic, which is the basis of ferroelectric behavior (Dawber *et al*., 2005).

1.3.3 Landau Theory of Phase Transition

The behavior of ferroelectric material can be described by thermodynamic principles which are clarified by Landau theory (ferroelectric mean-field theory). This theory provides a thermodynamic framework to describe phase transitions and polarization switching in ferroelectric materials. It describes the equilibrium of a system around a phase transition by using an order parameter (polarization) as the ferroelectricity can be defined by the non-polar to polar transition phase (paraelectric-ferroelectric) (Ong *et al.*, 2001).

The transition into the ferroelectric phase can be a first order phase transition or a second order phase transition. The former case is associated to a discontinuity of the value of polarization at temperature called Curie temperature (T_C).Through thermodynamic calculations, it is possible to describe the behavior of a ferroelectric crystal by considering the expansion of the Landau free energy as a function of the polarization (Segantini, 2023). If the one dimension case is considered, i.e. long uniform rod, the free energy (F) of a ferroelectric material is expanded as a function of the polarization (P) as:

$$F(P,T,E) = F_0 + \frac{1}{2}g_2P^2 + \frac{1}{4}g_4P^4 + \frac{1}{6}g_6P^6 - EP \qquad (1.5)$$

where F_0 is a reference energy, E is the applied electric field, and g_2, g_4, and $g_6$are phenomenological coefficients describing the material response.
The quadratic coefficient $g_2(T)$ varies linearly with temperature,

$$g_2(T) = \alpha(T - T_0) \qquad (1.6)$$

where $\alpha > 0$ and T_0 represents the Curie–Weiss temperature. The higher-order coefficients g_4 and g_6 are typically considered temperature-independent, with $g_6 > 0$ required to ensure that the free energy remains bounded at large values of P.

This sixth-order form often referred to as the Landau–Devonshire free energy has been widely used to describe the polarization behavior of classical ferroelectrics such as $BaTiO_3$ and $PbTiO_3$ (Lines & Glass, 1977; Chandra & Littlewood, 2007).

At thermal equilibrium, the spontaneous polarization corresponds to the stationary point of the free energy, where its first derivative with respect to P vanishes:

$$\frac{\partial F}{\partial P} = g_2 P + g_4 P^3 + g_6 P^5 - E = 0 \tag{1.7}$$

In the absence of an external electric field ($E = 0$):

$$g_6 P^5 + g_4 P^3 + g_2 P = 0 \tag{1.8}$$

Factoring out P gives:

$$P(g_6 P^4 + g_4 P^2 + g_2) = 0 \tag{1.9}$$

The trivial solution $P = 0$ corresponds to the paraelectric phase. Non-zero spontaneous polarization values satisfy:

$$g_6 P^4 + g_4 P^2 + g_2 = 0 \tag{1.10}$$

Since $P^2 \geq 0$, the spontaneous polarization is given by:

$$P = \pm \sqrt{\frac{-g_4 \pm \sqrt{g_4^2 - 4 g_6 g_2}}{2 g_6}} \tag{1.11}$$

Real polarization values occur when the discriminant $\Delta = g_4^2 - 4 g_6 g_2 \geq 0$. Among the possible solutions, the physically stable state corresponds to the lowest-energy equilibrium point of $F(P)$.

Each term in the Landau expansion plays a distinct role in defining the shape and evolution of the free-energy landscape. The quadratic term ($g_2 P^2$) determines the stability of the paraelectric phase and changes sign at the Curie temperature, marking the onset of ferroelectric order. The quartic term ($g_4 P^4$) dictates the nature of the phase transition:

A positive g_4 stabilizes the energy as g_2 becomes negative, resulting in a smooth, continuous emergence of spontaneous polarization (second-order transition). In contrast, a

negative g_4 introduces an instability around $P = 0$, requiring the higher-order sixth-order term (g_6P^6) which is always positive to maintain the overall stability of the energy function at large polarization magnitudes.

Finally, the linear term ($-EP$) accounts for the interaction between the polarization and the external electric field, leading to polarization switching and hysteresis under applied bias. Together, these terms define the overall curvature and symmetry of the free-energy profile and determine the equilibrium states accessible to the ferroelectric material. The sign of the quartic coefficient g_4 determines whether the ferroelectric transition is continuous or discontinuous:

- Second order (continuous) transition $g_4 > 0,\ g_6 \approx 0$: As the temperature decreases and $g_2(T)$ becomes negative, the single minimum of $F(P)$ at $P = 0$ gradually transforms into two symmetric minima at $\pm P_0$. Figure 1.5 illustrates this evolution of the free-energy profile: for $T > T_c$ (paraelectric phase) the curve shows a single minimum at $P = 0$, while for $T < T_c$ (ferroelectric phase) two equivalent minima appear at $\pm P_0$, representing the two stable polarization orientations. The spontaneous polarization increases smoothly according to the following equation, indicating a continuous transition at T_C:

$$P_s(T) = \sqrt{\frac{-g_2}{g_4}} = \sqrt{\frac{\alpha(T_0 - T)}{g_4}}, T < T_c, \tag{1.12}$$

- First-order (discontinuous) transition $g_4 < 0, g_6 > 0$: Here, the negative quartic term produces a region of metastability near $P = 0$, while the positive sixth-order term ensures that the free energy remains bounded for large P. As the temperature decreases, the non-zero minima become energetically favored, and at the Curie temperature $T_c > T_0$, the equilibrium polarization changes abruptly from zero to $\pm P_0$. This sudden jump in P_s signifies a first-order transition, characterized by a discontinuous polarization change and hysteresis typical of many perovskite ferroelectrics such as $BaTiO_3$.

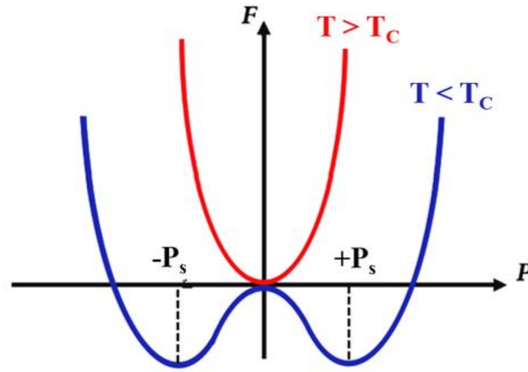

Figure 1.5: Free energy as a function of the polarization at T<T$_{\circ}$ and T>T$_{\circ}$ (Banerjee, 2022).

1.4 Theory of Ferroelectric Memory Switching

The behavior of ferroelectric capacitors can be further clarified by observing memory phenomena in hysteresis measurements. As shown in Figure 1.6, the ferroelectric capacitor displays a counterclockwise loop that reflects the response of dipole alignment as voltage is swept from zero to positive, back to zero, then to negative, and finally returning to zero (Evans, 1990). Key points on the loop such as A, B, and C represent the evolving internal charge state of the capacitor throughout the test.

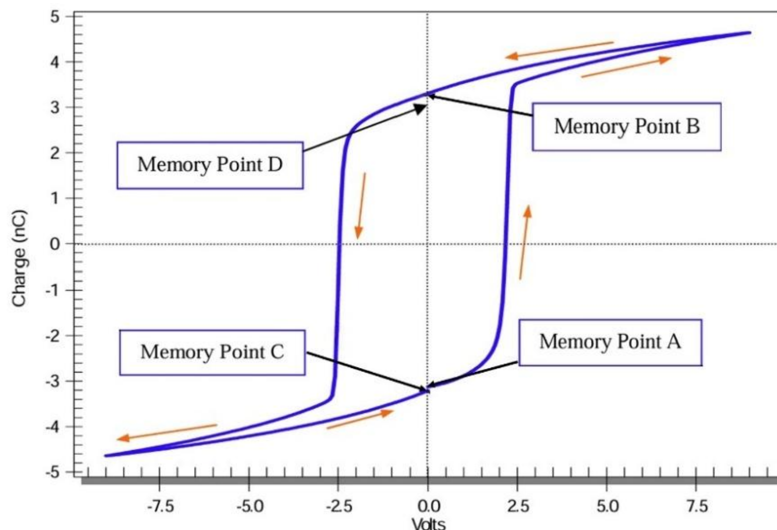

Figure 1.6: Memory response of a ferroelectric capacitor showing hysteresis loop behavior and evolution of charge state (Points A–D). Adapted from Evans (1990).

Point D indicates the partially decayed state of the capacitor when the applied voltage is reduced back to zero after reaching Point B. At this stage, the capacitor retains remanent polarization but undergoes a slight relaxation from B to D, reflecting the gradual decay of excess charge when held at zero bias. The orange arrows on the figure indicate the direction of the charge response along the voltage sweep. The presence of a "gap" between the start and end points of a sweep is attributed to temporary memory decay (Setter *et al*., 2006).

In a linear capacitor, the same amount of charge flows in and out during a full voltage cycle, leading to a return to the original uncharged state. However, in a ferroelectric capacitor, more charge is extracted when the field is applied than is restored upon returning to zero voltage. This charge imbalance indicates the presence of remanent polarization and is the core feature distinguishing ferroelectric capacitors from paraelectric and linear counterparts.

The ability of ferroelectric capacitor to retain a remanent polarization after the removal of an external electric field originates from the existence of dipolar domains within the ferroelectric material (Tagantsev *et al*., 2010). When an electric field is applied, the dipoles align along the field direction. Upon reversal of the field, the dipoles reorient, completing the polarization switch, switching begins only when the applied field exceeds the coercive field, reinforcing the threshold based, non-linear behavior. This constitutes the fundamental switching mechanism of ferroelectrics. The polarization-electric field (P–E) hysteresis loop reveals key material parameters:

- P_r: remanent polarization; the net polarization at $E = 0$.
- E_c: coercive fields; the minimum field required to reverse polarization.
- P_s: Saturation polarization when all domains are aligned.

These are depicted in Figure 1.7, which shows a typical P–E loop of a ferroelectric material.

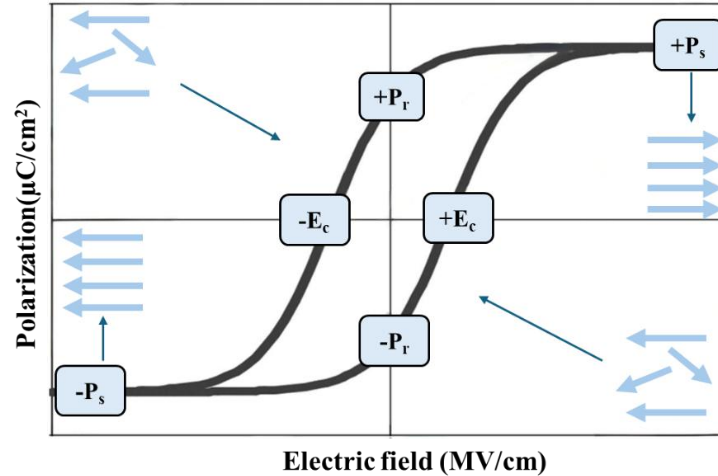

Figure 1.7: P–E hysteresis loop showing remanent polarization (±Pr), coercive field (±Ec), and saturation polarization (±Ps).

The theory of ferroelectric switching provides a framework for interpreting polarization behavior and serves as a foundation for understanding reliability and retention related phenomena like imprint, wake-up, fatigue, and aging; that are central to advanced ferroelectric material engineering.

1.5 Bragg's Law

The fundamental basis of X-ray diffraction lies in Bragg's law which defines the angular condition under which constructive interference occurs between scattered X-rays from parallel successive crystallographic planes. In other words, when the angle θ between the plane and the incident X-ray results in a path-length difference that is an integer multiple n of the X-ray wavelength, the scattered X-rays combine constructively. This is described by Bragg's law:

$$n\lambda = 2\,d\sin\theta \tag{1.13}$$

where:

n: is diffraction order.

λ: is the wavelength of incident X-rays (1.5406 Å for Cu Kα).

d: is the spacing between atomic planes.

θ: is the incidence angle.

Bragg's equation allows the determination of interplanar distances, and hence, identification of different crystalline phases. For example, orthorhombic HZO typically shows a peak near 30.5° in 2θ, which differentiates it from its tetragonal or monoclinic counterparts (Yoo *et al*., 2023). Figure 1.8 describes Braggs condition of X-ray diffraction.

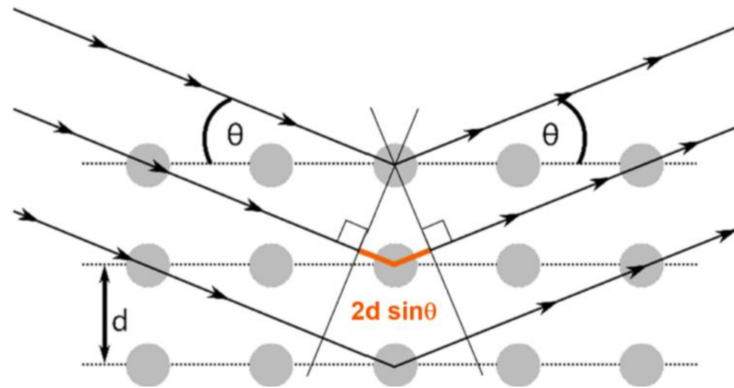

Figure 1.8: Schematic of Braggs condition (Harrington, 2023).

1.6 Degradation Effects in Ferroelectric Devices

As ferroelectric materials are increasingly integrated into advanced memory and logic applications, their long-term performance is influenced by a range of physical and electrical phenomena that emerge under real operating conditions. These effects, which arise from material imperfections and interfacial interactions, can gradually alter the polarization behavior and stability of devices. In ferroelectric capacitors, several such mechanisms including fatigue, imprint, aging, wake-up, and retention loss play a central role in determining endurance, switching uniformity, and data retention across extended use cycles.

Figure 1.9 highlights the architecture of a MFM capacitor and the P–E loop obtained from a 10 nm $Hf_{0.5}Zr_{0.5}O_2$ film. The capacitor's switching behavior is influenced by intrinsic and extrinsic factors including electric field, annealing, dopants, defects, thickness, oxygen vacancy migration, electrode interfaces, and mechanical stress. These

elements play key roles in shaping the hysteresis loop and polarization endurance during device operation (Zagni *et al*., 2023).

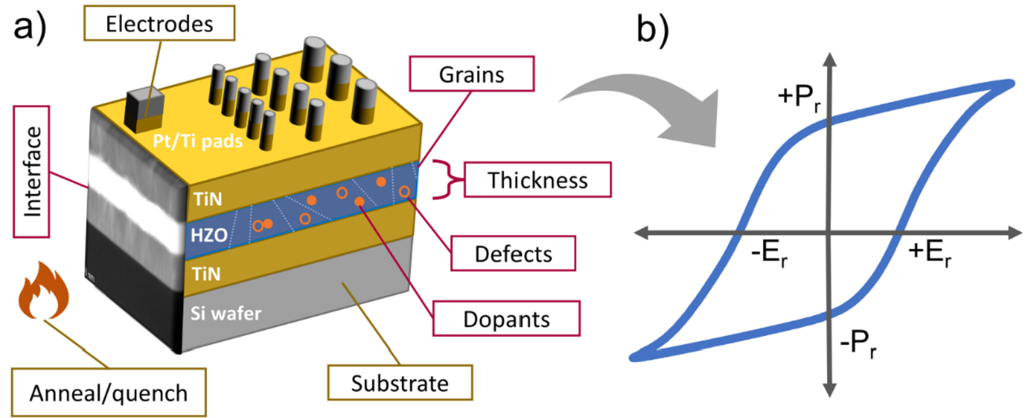

Figure 1.9: (a) Schematic of an MFM capacitor with contributing factors to polarization behavior. (b) Representative P–E loop of a 10 nm HZO film (Zagni *et al*., 2023).

A variety of instability mechanisms are observed in ferroelectric devices. These include polarization fatigue after repeated cycling, shifts in the P–E loop due to internal built-in fields (imprint), gradual reduction of switchable polarization over time (aging), and an initial increase in polarization during early cycling (wake-up). Figure 1.10 displays the effect of these phenomena over the hysteresis loops.

These effects collectively impact the reliability of ferroelectric response across different stress and time scales. While fatigue and aging are typically associated with defect accumulation and domain wall pinning, the wake-up effect is often linked to redistribution of oxygen vacancies and structural transformation from non-polar to polar phases. Imprint arises from asymmetric trapping of charges at the ferroelectric/electrode interface, leading to preferred polarization states and reduced symmetry in the hysteresis loop (Li *et al*., 2022; Zagni *et al*., 2023).

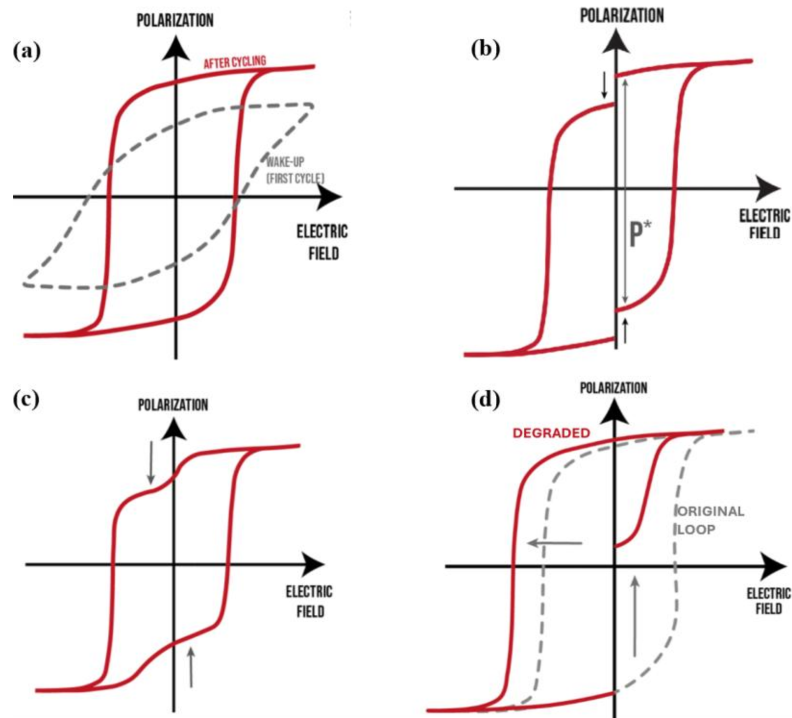

Figure 1.10: Common reliability phenomena in ferroelectric devices:(a) Wake-up effect, (b) Fatigue, (c) Ageing, and (d) Imprint effect. Adapted from (Hashemi, 2022).

1.7 Ferroelectric Materials: From Perovskites to Hafnium Oxide

Early implementations of ferroelectric capacitors, particularly in FRAM, were based on perovskite materials such as PZT and barium titanate ($BaTiO_3$). These compounds are characterized by the ABO_3 crystal structure, where the displacement of the B-site cation from the center of the oxygen octahedron produces a net electric polarization (Figure 1.11(a)). Perovskite-based materials offer high remanent polarization and stable switching characteristics; however, they suffer from limitations that make them unsuitable for advanced CMOS integration. These include high crystallization temperatures (> 600 °C), incompatibility with standard semiconductor processes, large physical thickness requirements, and lead-related environmental concerns (Mikolajick *et al*., 2020; Scott, 2000).

The need for scalable and CMOS-compatible ferroelectric materials led to a major shift in the field with the discovery of ferroelectricity in doped HfO_2 by Böscke *et al*. in

2011. Hafnium oxide is a fluorite-structured material widely adopted in the semiconductor industry as a high-κ dielectric. In fluorite structure ferroelectrics such as the ferroelectric orthorhombic phase in hafnium oxide, the oxygen ions can switch between two stable positions as represented in Figure 1.11 (b).

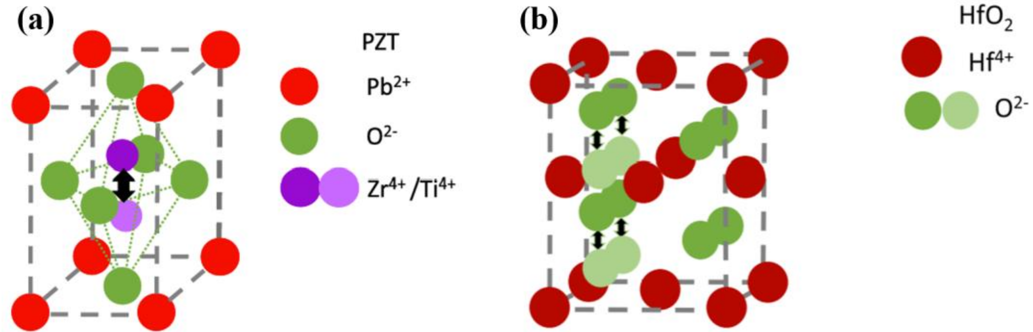

Figure 1.11: Schematic of a) a PZT crystal showing the two stable positions of a central Zr4+ or Ti4+ ion. b) hafnium oxide crystal indicating the switching of O2- oxygen ions in orthorhombic phase (Mikolajick *et al*., 2020).

The differences between PZT and HfO_2 in important material parameters have been considerably discussed in the literature, particularly in relation to their integration potential in ferroelectric devices. While PZT has long been the standard in ferroelectric memory technologies, its limitations in CMOS compatibility, high processing temperatures, and scaling have driven the search for the alternative materials. Hafnium oxide, in contrast, supports ferroelectricity in much thinner films and at a broader range of annealing temperatures, making it more suitable for modern device architectures.

Although both materials can achieve comparable remanent polarization, they differ significantly in properties such as coercive field strength, dielectric constant, and breakdown field. These distinctions, summarized in Table 1.1, highlight HfO_2's advantages for scaled and low-power applications (Kim *et al*., 2019; Müller *et al*., 2012). Hafnium oxide crystallize in different phases. Figure 1.12 illustrates the atomic arrangement of four principal crystallographic phases of HfO_2: cubic (c), tetragonal (t), monoclinic (m), and orthorhombic (o). The cubic phase represents the highest symmetry structure in the fluorite family and typically forms at high temperatures. It is centrosymmetric and therefore non-

ferroelectric. Upon cooling or due to certain constraints such as doping, this phase can transform into the tetragonal phase, which remains symmetric but becomes more elongated along one axis.

Table 1.1: Differences in the electrical and physical properties of PZT and HfO_2.

	PZT	HfO_2
Film thickness	>70 nm	1 nm -1μm
Annealing temperature	>600 °C	300-1050 °C
Remanent polarisation	20 – 40 (μC/cm^2)	1- 40 (μC/cm^2)
Coercive electric field	0.05 (MV/cm)	1-2 (MV/cm)
Breakdown electric field	0.5 -2(MV/cm)	4-8(MV/cm)
Relative Permittivity	≈ 1300	≈30

The monoclinic phase is the most thermodynamically stable at room temperature and dominates in bulk HfO_2; however, it is also centrosymmetric and non-polar. In contrast, the orthorhombic phase (space group $Pca2_1$) is non-centrosymmetric and supports spontaneous polarization, which is reversible under an external electric field. This phase is stabilized in thin films through doping (e.g., Zr, Si, Y) and size effects, and it is the origin of the switchable polarization observed in ferroelectric HfO_2 devices (Böscke *et al*., 2011). The red arrows in Figure 1.12 indicate the direction of polarization, emphasizing the bistability of the orthorhombic phase. Together, these phase transitions explain how HfO_2 becomes ferroelectric under nanoscale and engineered conditions (Banerjee *et al*., 2022).

1.7.1 HZO as a Ferroelectric Material

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Among doped HfO_2 systems, the alloy HZO has garnered particular attention. The inclusion of zirconium enhances the stability of the orthorhombic ferroelectric phase and improves film uniformity, resulting in stronger remanent polarization.

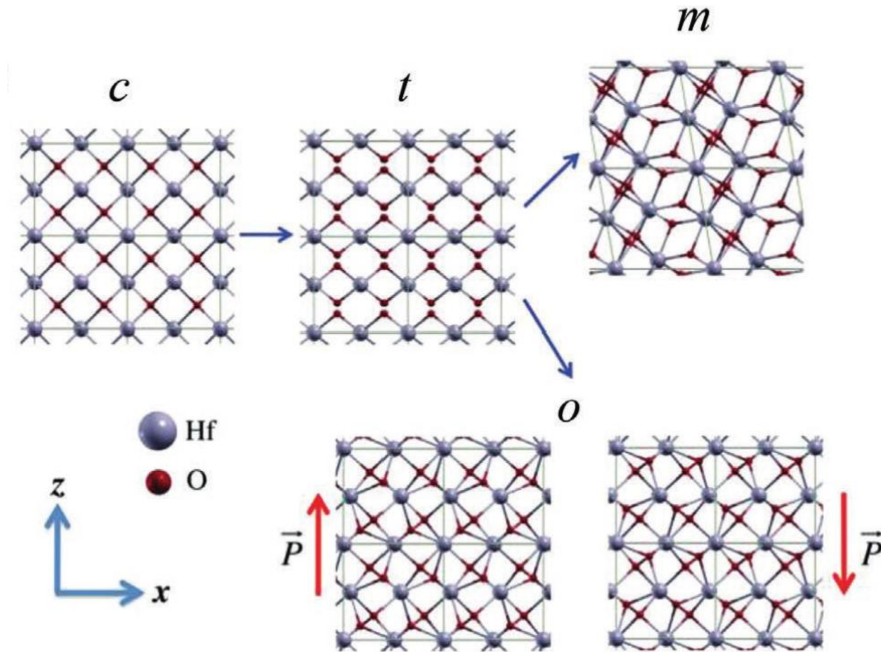

Figure 1.12: A schematic atomic view of the cubic, tetragonal, monoclinic and orthorhombic phases in HfO2 thin films (Banerjee *et al*., 2022).

Hafnium Zirconium Oxide demonstrates reliable switching at sub-10 nm thickness, ferroelectric field effect transistors (FeFETs), and tunnel junctions (FTJs) (Mikolajick *et al*., 2020; Jiang *et al*., 2021). Its performance at nanoscale thicknesses, coupled with its ability to conformally coat 3D structures, further strengthens its role in next-generation ultra-dense memory technologies. Zirconium was chosen in this study because its incorporation lowers the crystallization temperature of HfO_2, which promotes the formation of the ferroelectric orthorhombic phase during annealing. In addition, Zr shows chemical compatibility with Hf, allowing the formation of uniform solid solutions that enhance film quality and remanent polarization.

Recent research has highlighted the role of zirconium oxide (ZrO_2) as a critical alloying element in hafnium oxide-based ferroelectrics, owing to its close chemical and structural compatibility with HfO_2. When Zr is incorporated into the HfO_2, it forms a continuous solid solution between monoclinic and fluorite-derived structures (Mikolajick *et al*., 2020). One significant finding in this area is that Zr incorporation lowers the phase transition temperature from the monoclinic to tetragonal structure, facilitating the

stabilization of the metastable orthorhombic phase, which is essential for ferroelectric behavior in thin films (Müller *et al.*, 2012).

Structural and electrical characterization studies confirm that this phase behavior is composition-dependent. With increasing Zr content, a systematic evolution is observed from paraelectric HfO_2 to the ferroelectric $Hf_{1-x}Zr_xO_2$ and ultimately to the antiferroelectric ZrO_2phase (Müller et al., 2012). This transition is evident in both P–E loops and capacitance-voltage (C–V) profiles, which show a clear progression from narrow loops of paraelectric materials to open loops indicating ferroelectricity, followed by double hysteresis loops associated with antiferroelectric behavior as appears in Figure 1.13. The HfO_2 content of the $Hf_xZr_{1-x}O_2$ FE film decreases from left to right from $Hf_{0.7}Zr_{0.3}O_2$ to $Hf_{0.3}Zr_{0.7}O_2$.

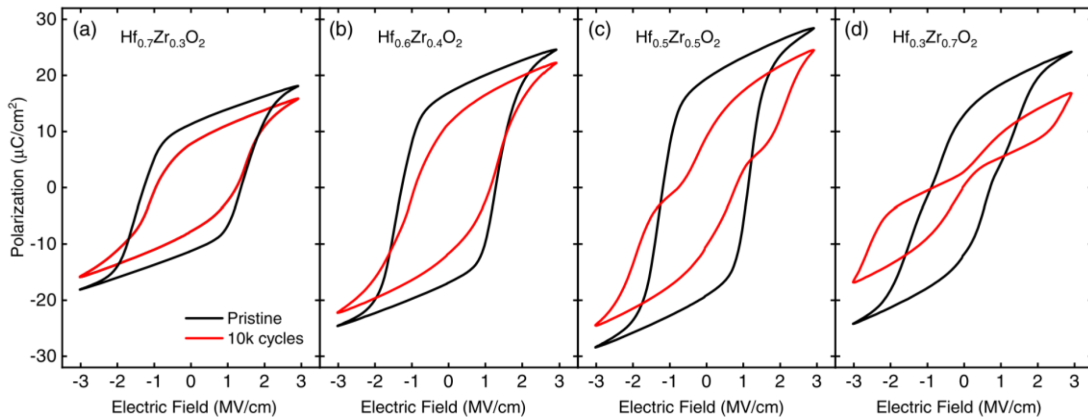

Figure 1.13: Polarization versus electric field measurements of MFM capacitors showing evolution of the loop with Hf and Zr content (Lederer., 2022).

This compositional tuning affects phase stability during post-deposition annealing. The tetragonal structure, formed during high-temperature deposition or annealing, transforms into the orthorhombic phase upon cooling, especially in stoichiometries near $Hf_{0.5}Zr_{0.5}O_2$. Hafnium-rich compositions tend to favor the monoclinic phase, while zirconium-rich variants crystallize predominantly in the tetragonal form (Starschich *et al.*, 2017). However, the 1:1 Hf:Zr ratio maximizes orthorhombic phase stabilization and thus remanent polarization, making this composition particularly favorable for FRAM devices.

Figure 1.14 illustrates the standard pressure phase diagram for the HfO_2–ZrO_2 system, emphasizing the thermodynamic stability of different crystallographic phases across compositions and temperatures. In bulk form, HfO_2 primarily adopts the monoclinic structure at room temperature, which is the most stable phase under equilibrium conditions. However, as temperature increases or as Zr content increases in the $Hf_{1-x}Zr_xO_2$ solid solution, phase transitions occur, progressing through tetragonal and cubic structures before reaching the liquid phase at high temperatures.

The diagram does not predict the polar orthorhombic ($Pca2_1$) phase responsible for ferroelectricity; this phase arises in thin films due to nonequilibrium factors such as surface energy effects and rapid thermal processing. For example, as mentioned previously, In $Hf_{1-x}Zr_xO_2$, the tetragonal phase can be stabilized at much lower temperatures than in the bulk, and subsequent cooling or annealing can induce a transition to the ferroelectric orthorhombic phase. These deviations from the standard phase diagram highlight the importance of kinetic and interface-driven effects in enabling ferroelectricity in hafnia-based materials (Hsain *et al*., 2022).

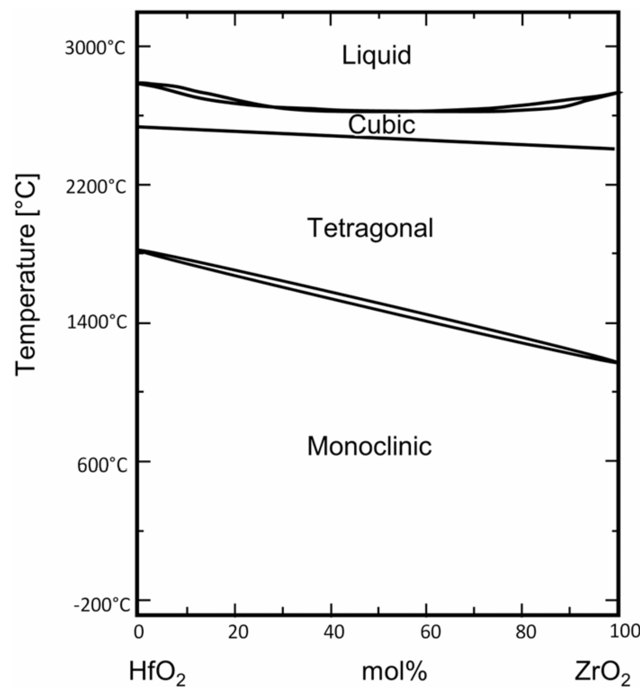

Figure 1.14: HfO_2-ZrO_2 standard pressure phase diagram (Hsain *et al*., 2022).

Chapter Two: Literature Review

The rapid development of hafnium oxide-based ferroelectrics, especially HZO, has paved the way for the realization of CMOS-compatible non-volatile memory devices. As memory technologies push toward higher density and lower power consumption, The 3D-MFM capacitor architectures based on TiN/HZO/TiN have emerged as a solution to overcome the limitations associated with planar (2D) designs particularly charge reduction, limited surface area, and reliability degradation at smaller nodes. This chapter reviews the state of the art in HZO-based ferroelectric capacitors, with particular attention to TiN/HZO/TiN devices and their 3D MFM architectures.

Earlier studies on 3D capacitor design by Burke *et al*. (2015), confirmed the feasibility of conformal deposition in high aspect-ratio trench geometries. The authors reported on structural and electrical properties of TiN/Al_2O_3/TiN capacitor structures in submicron 3D trench geometries with an aspect ratio of 30 as represented in Figure 2.1. Three layers for MIM stack were deposited using ALD in a single run at a process temperature of 250 °C. TiN top and bottom electrodes were deposited via plasma enhanced atomic layer deposition (PEALD) using a tetrakis(dimethylamino)titanium precursor. Both planar and 3D configurations of the studied structure were demonstrated over frequency ranges from 200 Hz to 100 kHz.

Although they used Al_2O_3 instead of HZO, their work validated the reliability and uniformity of 3D ferroelectric devices under cycling. 3D trench devices yielded capacitance densities of 36 fF/μm^2 and quality factors > 65 at low frequency (200 Hz), with low leakage current densities (< 3 nA/cm^2 at 1 V). The large capacitance density and low leakage of these all-ALD 3D devices shows promise for energy storage applications at low frequency and radio-frequency identification at intermediate frequency (125 kHz) (Burke *et al*., 2015).

The impact of 3D geometry has become central to HZO integration. Recently, Grenouillet et al. (2023) reported a study on 3D TiN/HZO/TiN capacitors fabricated in high-aspect-ratio via structures. Their results demonstrated up to 35% enhancement in remanent

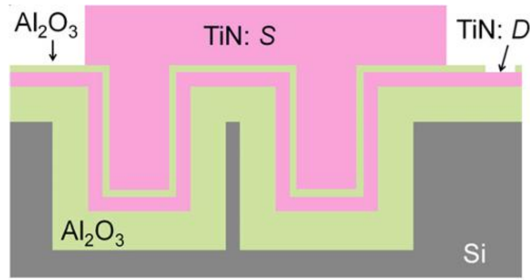

Figure 2.1: Side-view schematic of a trench array (Burke *et al*., 2015).

polarization compared to planar devices, attributable to increased effective surface area and improved electric field distribution. Forming gas annealing (FGA) further enhanced device endurance while preserving polarization behavior. Figure 2.2 (a) Displays cross-section schematic and scanning electron microscope (SEM) image of MFM stack deposited on patterned vias. Figure 2.2 (b) displays comparison of $2P_r$ values vs planar geometry (Grenouillet *et al*., 2023).

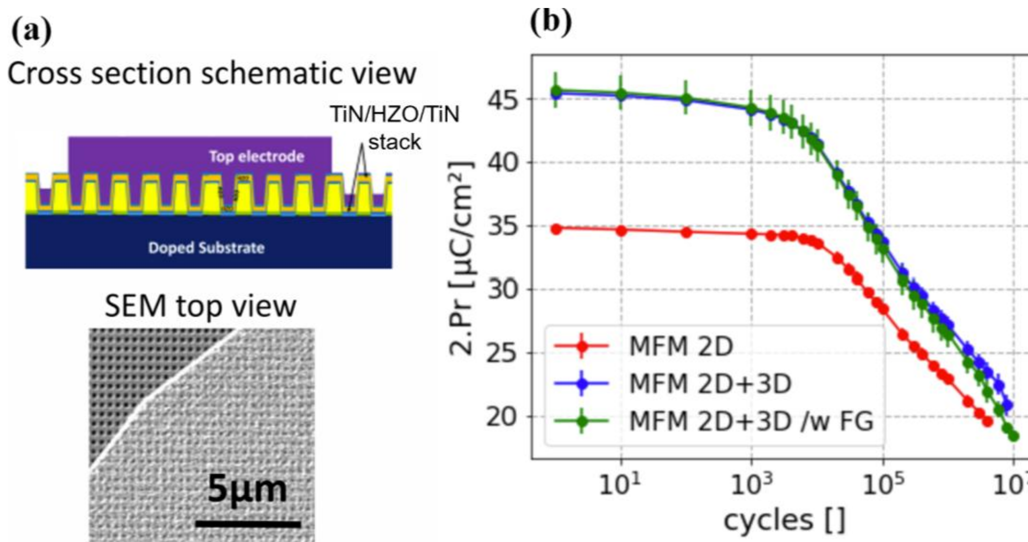

Figure 2.2: (a) Cross section schematic and SEM views of MFM stack deposited on patterned vias, leading to 2D+3D shaped MFM capacitors, and (b) Evolution of $2P_r$ measured with 4MV/cm, 10kHz PUND along 3MV/cm bipolar field cycling (Grenouillet *et al*., 2023).

Comparing these developments with the current study, the influence of aspect ratio becomes especially significant. The earlier studies did not provide analysis of how the aspect

ratio itself influences ferroelectric properties. However, the present study explicitly investigates the impact of aspect ratio on TiN/HZO/TiN capacitors fabricated in patterned 3D geometries. GIXRD and PUND measurements performed in this work showed enhanced peak intensity and remanent polarization with increasing aspect ratio. The polarization values reached in this study are consistent with and in some cases exceed, those reported in earlier 3D designs, particularly under optimized annealing and deposition conditions. These similarities reinforce the relevance of structural design and dimensional scaling in HZO-based ferroelectric integration.

To optimize HZO devices performance at nanoscale dimensions, researchers have demonstrated that stress and electrode interface engineering are key mechanism for stabilizing the non-centrosymmetric orthorhombic phase in HZO. For example, A study by Kim et al. (2017) revealed that the deposition of TiN electrodes before thermal treatment induces tensile stress on the HZO layer, suppressing the formation of the non-ferroelectric monoclinic phase and promoting the orthorhombic ferroelectric phase.

Their TiN/HZO/TiN capacitors achieved remanent polarization values of ~ 45 $\mu C/cm^2$ at annealing temperatures as low as 400 °C. It was concluded that an annealing process (as low as 400 °C for 1min) is required and should be performed after TiN top electrode (90 nm or higher) deposition at room-temperature for the 10 nm HZO crystallization to exhibit a non-centrosymmetric o-phase. This prove the effectiveness of stress-induced crystallization in enhancing performance under a low thermal budget (Kim *et al*,. 2017). The schematic architecture of the studied structure and their Polarization results are displayed in Figure 2.3.

In another study, Hashemi *et al*. (2021) investigated HZO stacks using single-target sputtering and demonstrated promising ferroelectricity and low leakage characteristics. Their findings emphasized how annealing conditions can influence the remanent polarization and dielectric constant. The current-voltage and dielectric constant – voltage characteristics in Hashemi's study are displayed in Figure 2.4. Single-target sputtering method proved suitable for large-area applications while preserving material integrity. Their findings confirmed the potential of sputtered HZO for commercial non-volatile memory integration.

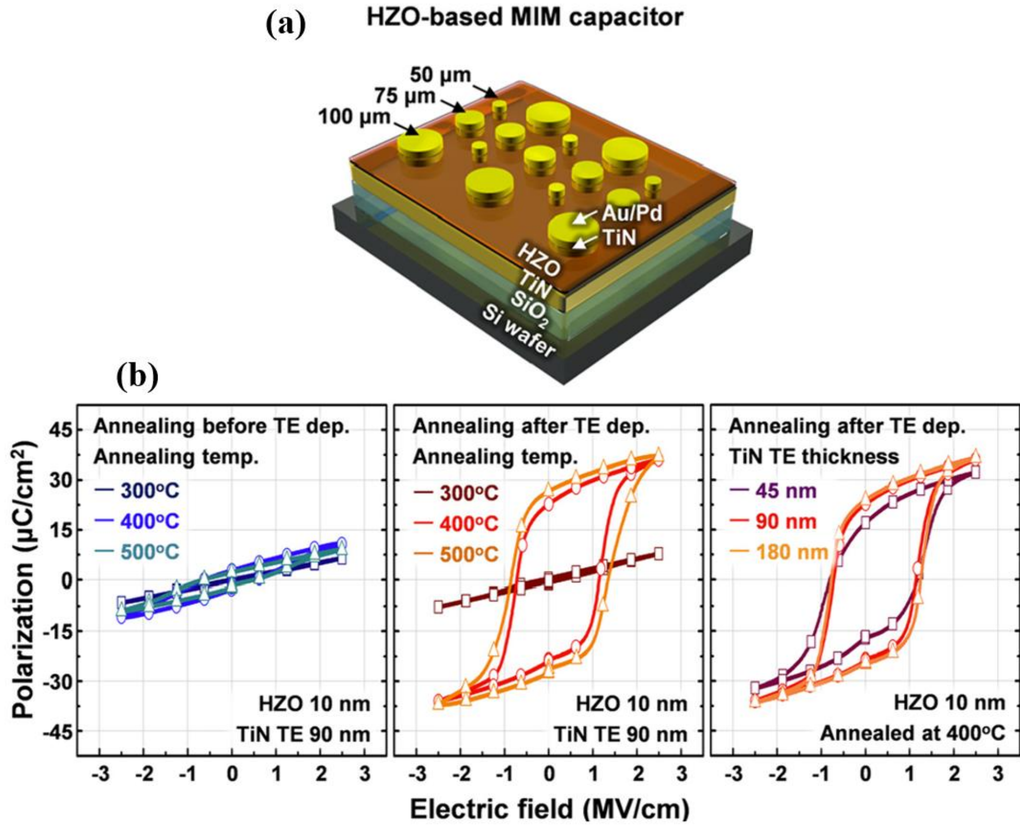

Figure 2.3: (a) Schematic illustration of the HZO-based MIM capacitors. (b) Polarization-electric field hysteresis curves after wake-up field cycling before and after annealing with and without a TiN top electrode (Kim *et al*,. 2017).

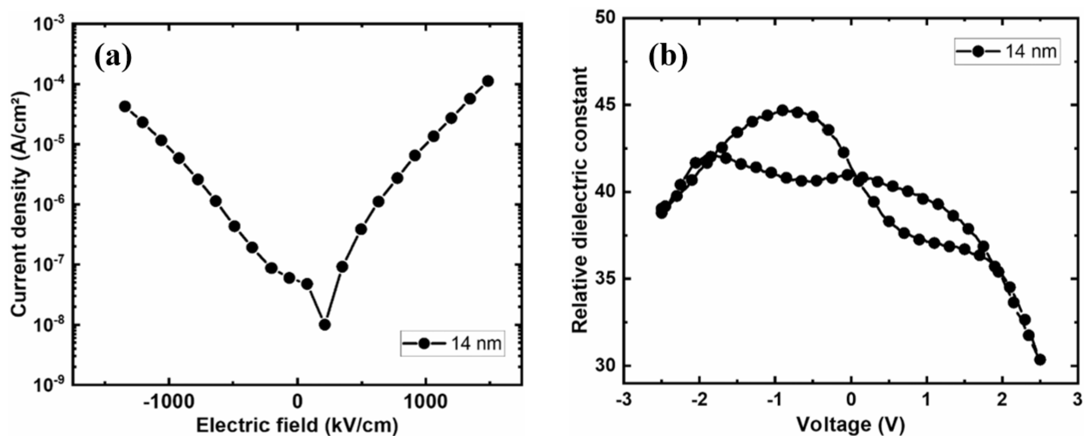

Figure 2.4: (a) Current density vs. electric field of TiN/HZO(14 nm)/TiN stack annealed at 650 °C for 1 min. (b) Relative dielectric constant vs. voltage for the same structure and conditions (Hashemi *et al*., 2021).

Study on the effect of annealing temperature by Lee *et al*. (2021) using no-atmosphere processing (NAP) deposition technique revealed that annealing at (400 - 800)°C without breaking vacuum improved crystallinity and polarization ($2P_r$ ~ 54.2 μC/cm²) with largest orthorhombic phase fraction 2Pr¼. This increase is explained by the absence of interfacial passive layers created in the NAP deposition. In addition an increase in the concentration of defects such as carbon, nitrogen, and oxygen vacancies within HZO layer during RTA processing. These results highlight how annealing conditions influence HZO performance (Lee *et al*., 2021). The electrical and structural results are represented in Figure 2.5.

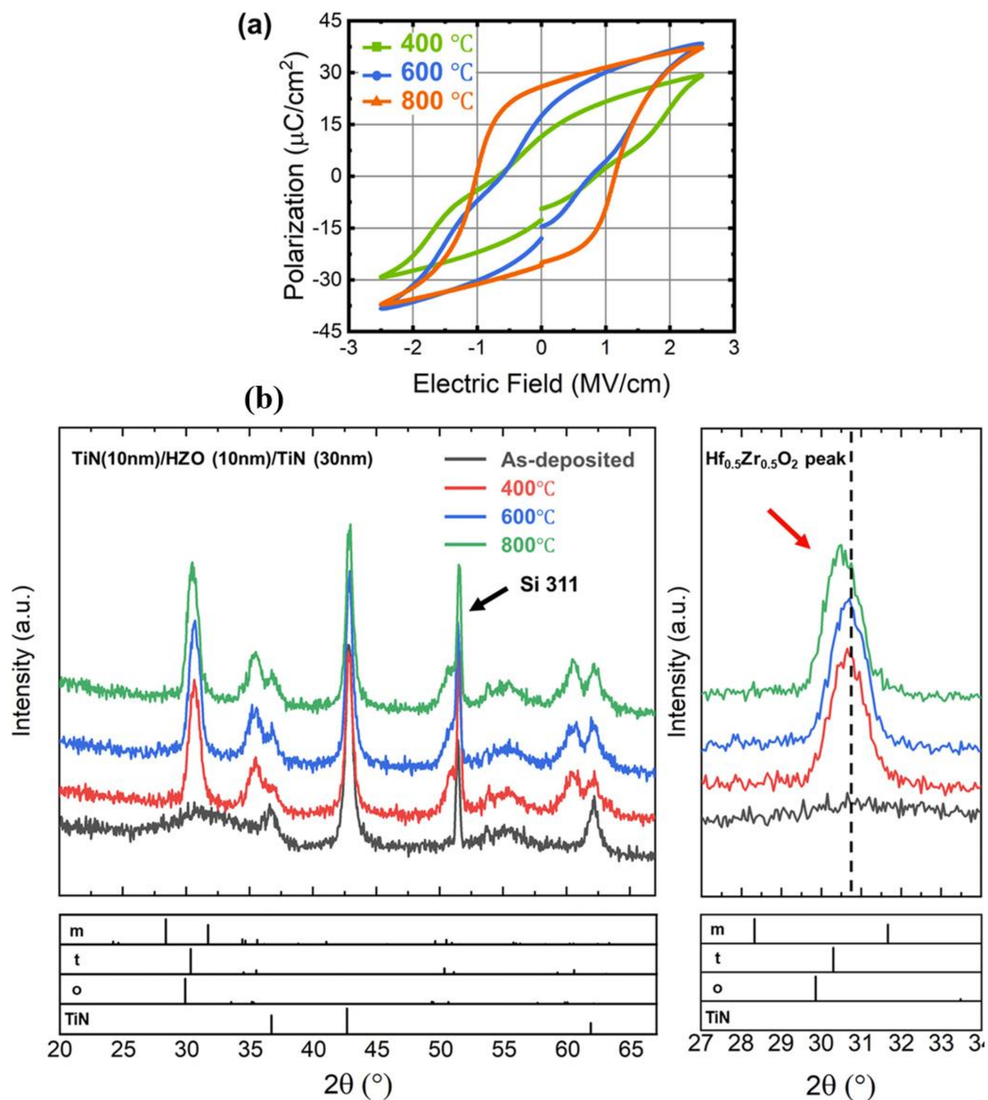

Figure 2.5: (a) P–E hysteresis loop. (b) GIXRD patterns of TiN(10nm)/HZO(10nm)/TiN(30nm) after various annealing treatments (left) and in the magnified 2θ range of 27° to 34° (right) (Lee *et al*., 2021).

Complementing this (Liang *et al*, 2021) demonstrated the effect of annealing temperature (400°C- 600°C) on ferroelectric properties and reliability of ALD deposited TiN/HZO/TiN capacitor stack. The sample annealed at 600°C shows high remanent polarization of 52.9 $\mu C/cm^2$ and excellent endurance performances with higher than 10^{11} cycles at 3 V without breakdown as shown in Figure 2.6. It is suggested that higher annealing temperature can enhance the crystalline quality as well as interface in the ALD deposited TiN/HZO/TiN capacitor (Liang *et al*., 2021).

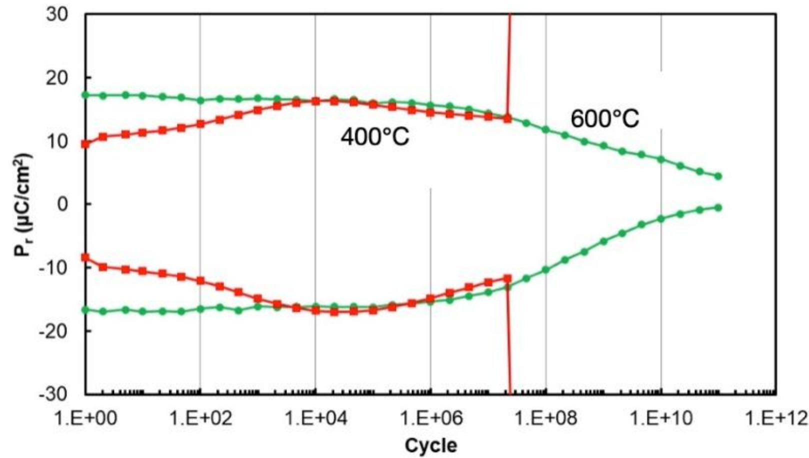

Figure 2.6: The endurance of 400°C and 600°C PMA (Liang *et al*., 2021).

Thickness dependence of dielectric and ferroelectric behavior was detailed by Puqi Hao *et al*. The authors analyzed Polarization–voltage (P-V) loops for HZO layers ranging from 5 to 23 nm which are displayed in Figure 2.7. Thinner films exhibited degraded dielectric properties and faster polarization switching. It is revealed that the degradation of dielectric constant with frequency and the dielectric loss value become faster and larger with decreasing the thickness, respectively. Based on deep analysis of polarization switching kinetics, it is found that the polarization switching speed, fundamentally governed by grain size, is responsible for thickness dependence of evolutions of dielectric responses with frequency (Hao *et al*., 2023).

To further reduce thermal budget, simulations by Liu *et al*. (2024) display electric-field- induced crystallization as an effective technique for enhancing crystallinity and

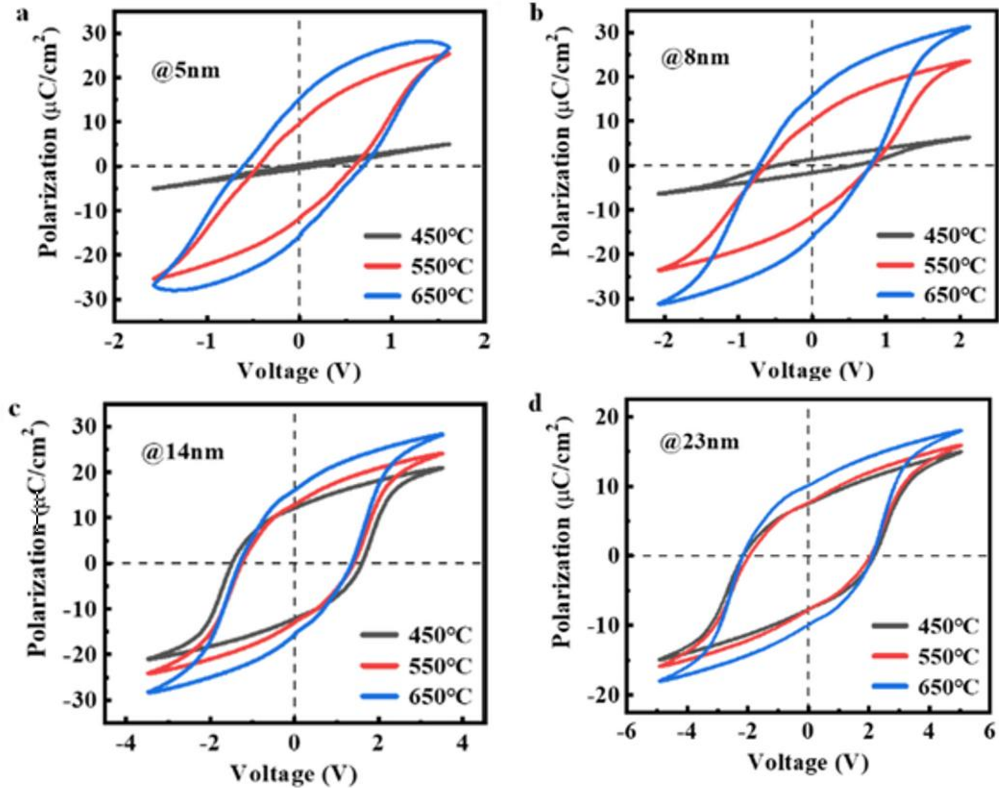

Figure 2.7: P–V hysteresis loops of the a) 5-nm-, b) 8-nm-, c) 14-nm-, and d) 23-nm-thick HZO annealed from 450 °C to 650 °C, respectively (Hao *et al*., 2023).

polarization without high temperature annealing. Their work modeled the gradual nucleation and domain evolution in HZO thin films under electric pulses, achieving polarization saturation values up to 32 μC/cm² as shown in Figure 2.8. This supports the concept of using electric activators to achieve high quality ferroelectric layers in 3D configurations, which is particularly helpful for back-end-of-line integration where thermal budgets are limited Electric field induced (Liu *et al*., 2024).

In other study, Saini et al studied the cause of wake-up effect in HZO capacitors using non-destructive methods that probe statistically significant sample volumes. Synchrotron X-ray diffraction reveals a concerted shift in HZO Bragg peak position as a function of polarization switching cycle number in films prepared under conditions such that they exhibit extremely large (~3000%) wake-up. Piezoresponse force microscopy measurements are utilized to visualize domain switching with wake-up.

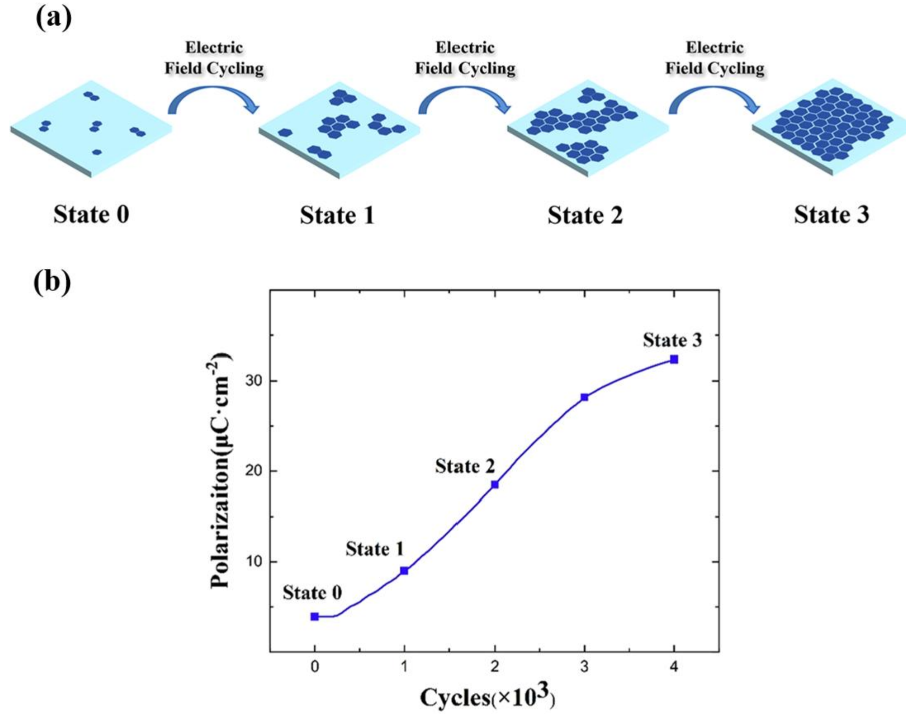

Figure 2.8: (a) Schematic of crystallinity in different states. (b) The polarization versus applying electric field cycles. (Liu *et al*., 2024).

Polarization - voltage hysteresis loops for ALD 250 °C and ALD 200 °C samples are displayed in Figure 2.9 (a) and (b) respectively. The combination of these observations clearly demonstrates that wake-up is caused by a field driven phase transformation of the tetragonal phase to the metastable ferroelectric orthorhombic phase during polarization switching of HZO capacitors (Saini *et al*., 2023).

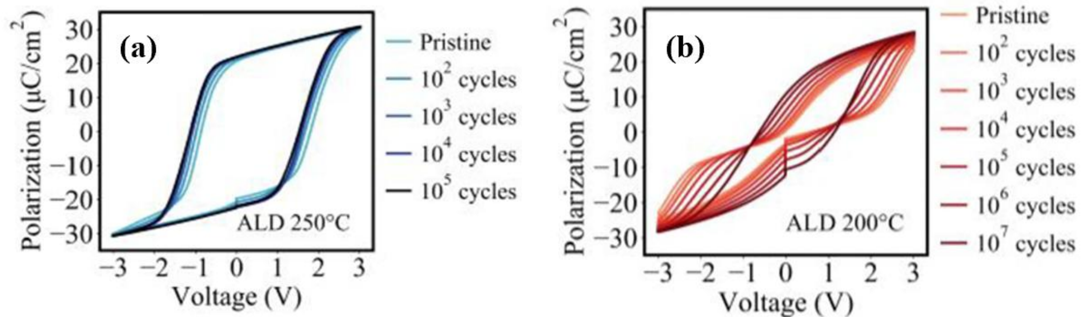

Figure 2.9: PV hysteresis loops for (a) ALD 250 ◦C (b) ALD 200 ◦C samples respectively (Saini *et al*., 2023).

Chapter Three: Methodology

This chapter describes and clarifies the experimental methods and characterization technique used to study the 3D HZO-integrated capacitor. It is organized into three main parts: The first part details the deposition and fabrication processes performed to manufacture the wafers and fabricate the samples. The second part focuses on the physical and structural characterization of the samples. Finally, the third part presents the electrical characterization methods used to evaluate the device performance.

3.1 Deposition and Fabrication Techniques

The studied samples were obtained by cutting 300 mm-integrated HZO MFM capacitor wafers, manufactured at the Laboratory for Electronics and Information Technology of the French Alternative Energies and Atomic Energy Commission (CEA-LETI) into 2x2 cm samples. These capacitors were prepared on highly doped n-type (n++) silicon substrate which can be used as bottom electrode of the capacitor from the back surface of the samples. 35nm-thick SiN Layer was deposited on this substrate at 320 °C. Then a layer of SiO_2 with thickness of 300 nm or 500 nm was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) at 350 °C.

To design the 3D structure, selected areas of the dielectric stacks were etched down to the substrate. Following this, the layers of the MIM capacitor were deposited. A 10 nm-thick TiN bottom electrode was deposited by CVD at approximately 380 °C. The HZO layer, with thicknesses ranging from 6 nm to 10 nm, was deposited by ALD at around 300 °C, maintaining a 1:1 Hf:Zr ratio. The top electrode was then deposited by CVD, consisting of a 5nm TiN layer followed by tungsten (W) filling, also at approximately 380 °C.

A uniform Post-Deposition Annealing (PDA) process was applied to all HZO thicknesses, consisting of annealing at 400 °C for one hour. This step was performed prior to the final lithography and etching processes used to define rounded MFM capacitors.

Figure 3.1 presents a 3D schematic of the 3D HZO integrated capacitors visualizes geometry of the 3D capacitor design and showing the thicknesses of top and bottom electrods in addition to the ferroelectric HZO layer.

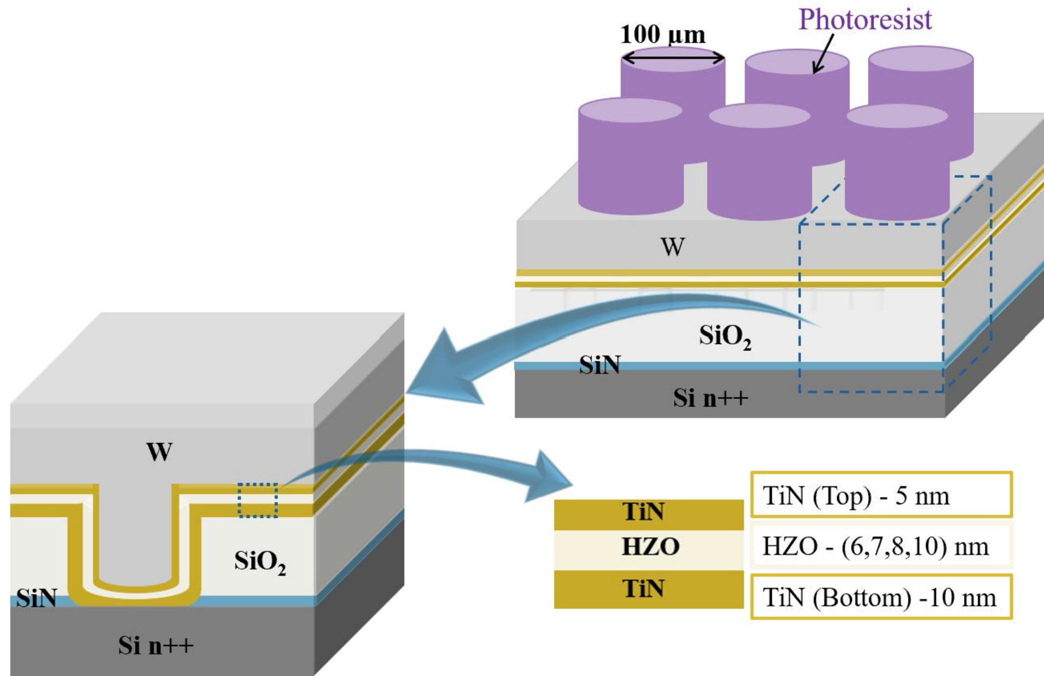

Figure 3.1: 3D cross section schematic of the 3D HZO-integrated capacitors.

Figure 3.2 presents a 2D schematic showing thicknesses of all the deposited layers, in addition to the geometry of the 3D capacitor design, including the width of the etched semi-cylindrical holes and the distances between them in both the x- and y-dimension. The thickness of SiO_2 is varied between two values: 300 nm and 500 nm. SiO_2 thickness determine aspect ratio value of the 3D structure which is defined as the ratio between the height and the width of the hole. The width of the hole is 280 nm, but for simplification it is approximated to 300 nm. Hence, two groups of samples are defined depending on SiO_2 thickness: samples with aspect ratio equal 300/300 and samples with aspect ratio equal 500/300. The deposition techniques and fabrication methods employed are detailed in the following subsections.

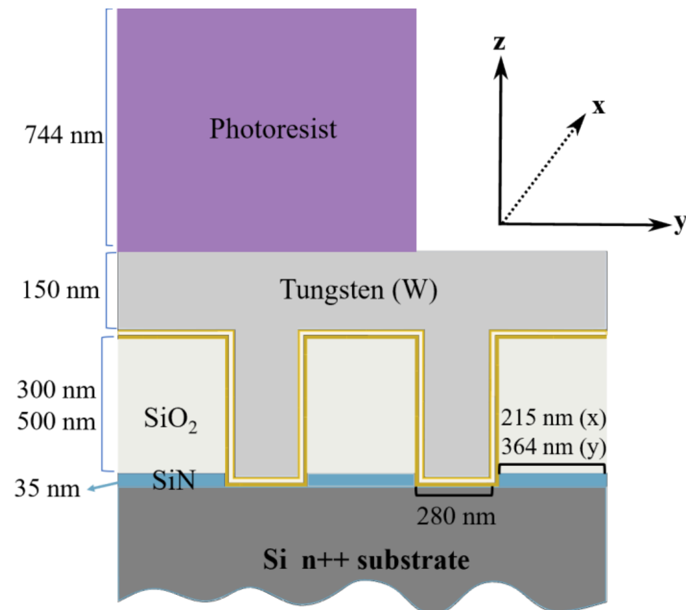

Figure 3.2: 2D cross section schematic for 3D HZO integrated capacitors.

3.1.1 Chemical Vapor Deposition Technique (Growth of TiN Electrodes)

Chemical vapor deposition is a widely employed technique for depositing thin films of materials, including TiN (Lee et al., 2023). This process involves the chemical reaction of precursors in vapor phase to form a solid film on a substrate. CVD is favored for its ability to produce high-purity, uniform coatings with brilliant conformality, making it suitable for complex geometries and high aspect-ratio structures (Rebenne & Bhat, 1994). The process parameters, such as temperature, pressure, and precursor selection, can be precisely controlled to tailor the film's properties.

For the studied structure, both the top and bottom TiN electrodes were deposited using thermal CVD at a substrate temperature of 380 °C. The bottom electrode was deposited directly onto SiO_2 layer, while the top electrode consisted of a TiN layer followed by W filling, both deposited at the same substrate temperature.

Titanium nitride deposition by CVD is influenced by several experimental parameters. The selection of precursors plays a fundamental role in determining the

composition and properties of the deposited film. Commonly used precursors for TiN deposition include titanium tetrachloride ($TiCl_4$) and ammonia (NH_3), which react to form TiN while releasing hydrogen chloride (HCl) as a byproduct (Abadias, 2008). In addition, maintaining an appropriate substrate temperature is essential for ensuring high film quality.

For the studied structure, a temperature of 380 °C was employed to optimize deposition. Another important parameter is the deposition pressure, as operating under reduced pressure enhances film uniformity and minimizes undesirable gas phase reactions. Typical pressures range between 10 and 100 Torr (Wagner et al., 2008). The deposition time and growth rate are also critical considerations, as they determine the final film thickness. Growth rates for TiN via CVD typically range from 5 to 20 nm/min, depending on specific process conditions (Rebenne & Bhat, 1994).

Titanium nitride is a preferred material in MIM capacitor structures due to its high electrical conductivity, excellent thermal and chemical stability, and strong diffusion barrier properties. In the context of the 3D HZO-integrated capacitors investigated in this study, the conformal deposition achieved through CVD is especially important for ensuring uniform electrode coverage over etched structures with high aspect ratio. Furthermore, the integration of W as a filler atop the TiN top electrode enhances both electrical conductivity and mechanical integrity (Lee *et al*., 2023).

3.1.2 Atomic Layer Deposition Technique (Growth of HZO Layers)

Atomic layer deposition is a highly controlled thin-film deposition technique that belongs to broader category of CVD methods. While both ALD and conventional CVD rely on vapor-phase chemical reactions with the substrate surface (Leskelä & Ritala, 2002), ALD is distinguished by its self-limiting, sequential surface reactions. This unique mechanism enables atomic-scale control over film thickness, exceptional uniformity, and conformality, particularly over complex topographies and high-aspect-ratio structures (Gupta et al., 2022). These attributes make ALD especially suitable for fabricating 3D integrated ferroelectric devices, where uniform and pinhole-free films are essential.

The ALD process is typically carried out at lower temperatures (50-300 °C) compared to conventional CVD, reducing thermal stress and limiting interfacial diffusion. It consists of alternating exposure and purge steps that isolate each half-reaction, thereby eliminating unwanted gas-phase reactions and ensuring layer-by-layer growth with precise thickness control (George, 2010). The mild thermal budget of ALD also helps preserve the integrity of underlying layers (Miyata *et al*., 2021). The key experimental parameters influencing ALD growth include:

- Type of precursors
- Deposition temperature
- Exposure and purge times
- Growth rate
- Final film thickness and stoichiometry

For the investigated structures, $Hf_{0.5}Zr_{0.5}O_2$ layers with thicknesses ranging from 10 nm down to 6 nm were deposited at 300 °C using thermal ALD. The precursor chemistry involved Tetrakis (ethylmethylamino) hafnium (TEMAHf) and Tetrakis (ethylmethylamino) zirconium (TEMAZr) as Hf and Zr sources, respectively, while H_2O was used as the oxidant. These precursors enabled precise control over the Hf:Zr atomic ratio, maintained at 1:1- an important factor influencing the ferroelectric phase stability of HZO (Xiao *et al*., 2020). The typical growth rate is approximately 1 Å per cycle, allowing highly accurate film thickness control. Following deposition, post-deposition annealing at 400 °C for 1 hour was employed to enhance crystallinity and promote ferroelectric properties.

Atomic layer deposition is a versatile platform capable of depositing a wide range of materials, including oxides, nitrides, sulfides, and elemental films. The selection of precursors depends on their physicochemical properties, such as thermal stability and vapor pressure, as well as their influence on the electrical performance of the resulting material. Figure 3.3 provides a broad overview of the types of materials accessible by ALD.

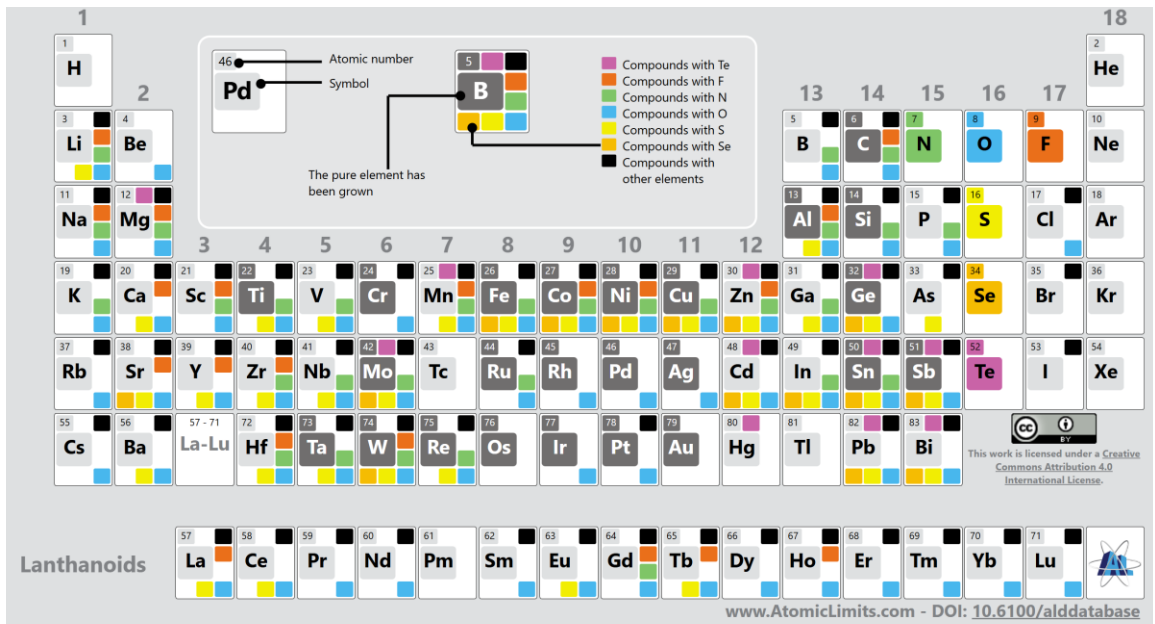

Figure 3.3: Overview of the materials that can be grown by ALD (2019). Adapted from *Atomic Limits ALD Database* (van Ommen & Mameli, 2019).

The Principle of ALD relies on irreversible and saturating, separated gas-solid reactions of normally at least two compounds, which are repeated in a cyclic manner. One ALD cycle involves typically of four steps, as schematically illustrated in Figure 3.4: first gas-solid reaction, i.e., chemisorption reaction, of the first reactant (Precursor A), typically of a metal reactant (Step1); purge or evacuation to remove the unreacted precursor and gaseous by-products (Step 2); second gas-solid reaction, i.e., chemisorption reaction, of the second reactant (Precursor B), typically of a non-metal reactant (Step 3); and again purge or evacuation to remove the unreacted precursor and gaseous by-products (Step 4). (Please note that the compounds used to deposit film by ALD are often called precursors or reactants. Sometimes, a distinction is made to call the metal compound "precursor" and the non-metal compound "reactant."

The HZO layers of the studied capacitors were deposited at CEA-LETI using industrial-scale ALD tools. However, Figure 3.5 displays a photograph of the laboratory-scale ALD system (FlexAL™ reactor developed by Oxford Instruments) available at BCAI clean room (Building for Characterization and Integrated Analysis) CIME-Nanotech,

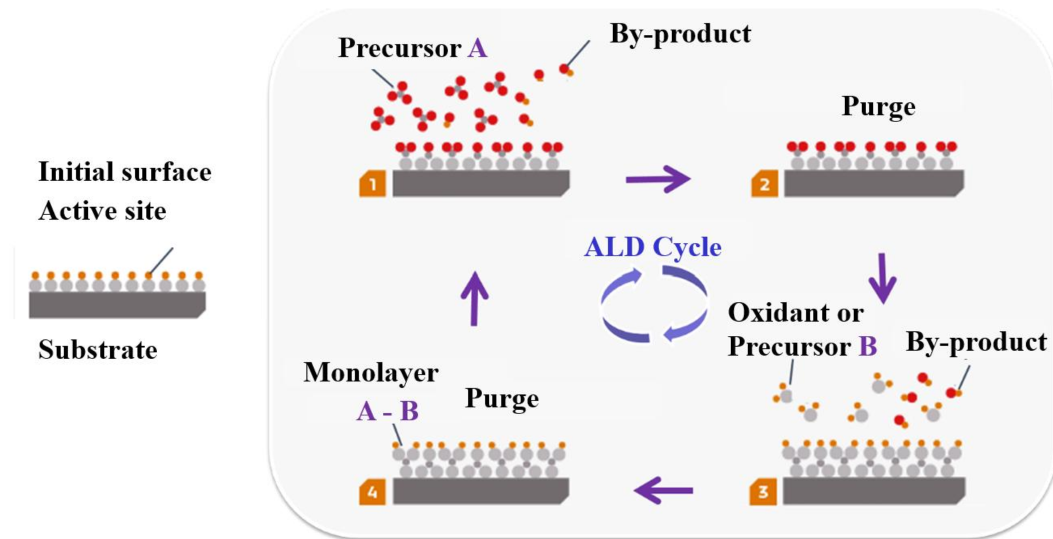

Figure 3.4: Schematic illustration of one ALD reaction cycle. Adapted from a diagram on ASM.com.

where part of the training related to this work was performed. The main components of the system include:

1) Main Process Chamber: Where the actual deposition takes place; the sample is loaded and subjected to sequential precursor pulses under vacuum.
2) Load Lock Chamber: A small isolation chamber that allows sample transfer without compromising vacuum conditions in the main process chamber.
3) Precursor Cabinet: Houses the precursor bottles, mass flow controllers (MFCs), and carrier gas lines, enabling precise and automated delivery of reactants.
4) In situ Ellipsometer: An integrated optical system used to monitor film thickness and growth per cycle in real time.

The FlexAL reactor is optimized for both thermal and plasma-enhanced ALD, offering flexibility in process conditions and material selection and ensuring high-quality films suitable for ferroelectric applications.

Figure 3.5: ALD Flexal reactor developed by Oxford equipment's Located at BCAI clean room in CIME.

3.1.3 Photolithography

To define the electrode geometry, photolithography was performed using a Nikon M300 VIA INF system. A 400 nm-thick positive TOK7052 photoresist and an 82 nm anti-reflective coating (BARC AR19) were spin-coated onto the tungsten surface. Photolithography is a microfabrication technique that enables pattern transfer onto a substrate by using a light-sensitive photoresist layer exposed to ultraviolet light through a mask, allowing selective material removal (Madou, 2011).

Figure 3.6 (a) displays 300 mm wafer of 3D HZO integrated capacitor and shows the shape of the used lithography mask which include identical squares arranged in regular manner, inside each of these squares, There are 40 × 40 arrays of identical circles (actually cylinders) each with a 100 µm diameter, serving as protective masks for the subsequent etching step. The number of devices in each square was detected. Figure 3.6 (b) displays schematic square of 40 × 40 arrays of circles. Each of these circle can be tested electrically as separated pristine device. Figure 3.6 (c) shows number of cylindrical photoresist

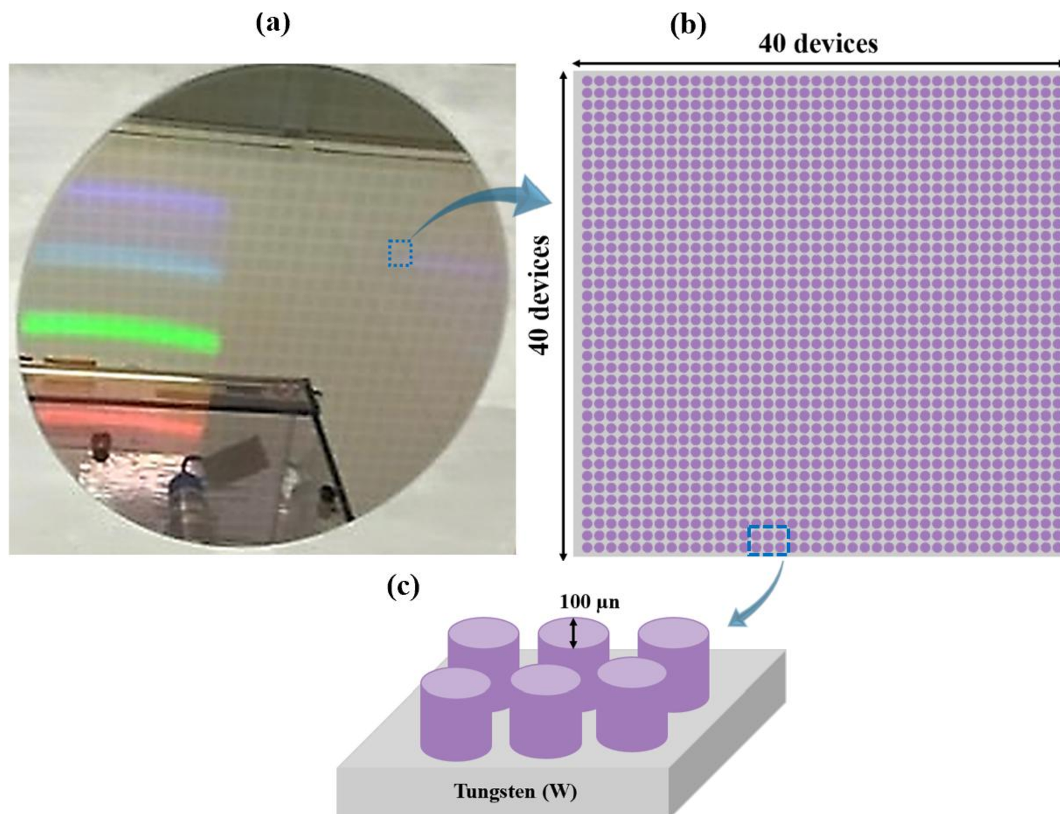

Figure 3.6: (a)Wafer of 3D HZO integrated capacitor. (b) Scheme display 40 × 40 arrays of circles in one square. (c) cylindrical photoresist on W layer.

As an example of such equipment for photolithography process, Figure 3.7 shows photolithography mask aligner in BCAI clean room in CIME which is used in photolithography process.

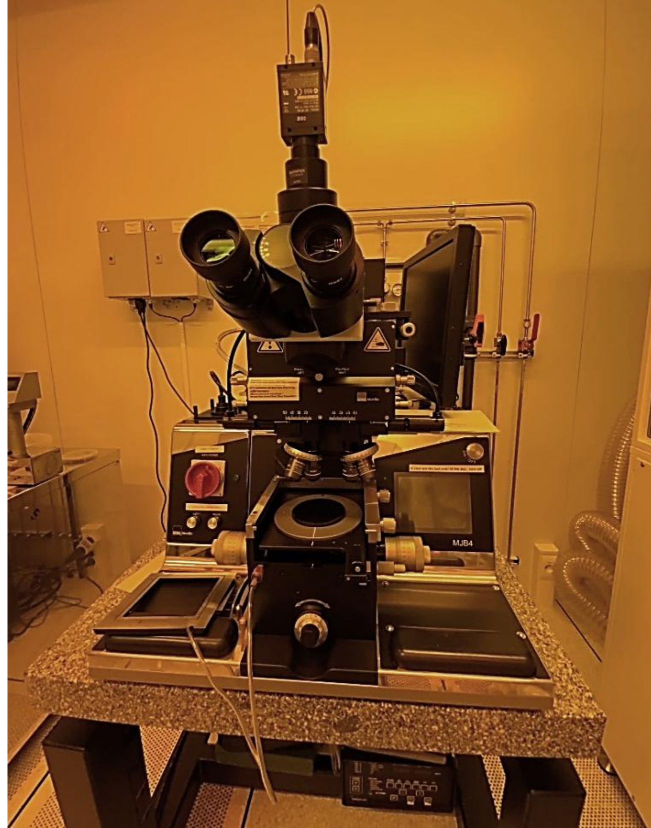

Figure 3.7: Lithography Mask aligner.

3.1.4 Etching: Inductively Coupled Plasma Reactive Ion Etching

Following lithography, inductively coupled plasma reactive ion etching (ICP-RIE) was performed to remove the unprotected W areas and electrically isolate individual MFM capacitors. During the etching, low-speed etched photoresist cylinders were used as a mask to protect W areas (cylinders with a diameter of 100μm); the W layer between these photoresist cylinders was etched.

Inductively coupled plasma reactive ion etching is a highly anisotropic dry etching technique that employs a high density plasma source to generate reactive particles, which interact with the surface to remove material in a controlled manner without excessive substrate damage (Mutsukura & Turban, 1990). The main significant parameters for ICP etching is etching time in addition to etchant material employed in the process. To

determine when and at each layer, the etching should be stopped, it is important to ensure complete removal of the 150 nm-thick tungsten layer and confirm that the devices are separated accurately avoiding excessive over-etching into inner layers.

Determining the time of etching for this study and the etchant was done after many experiments and after analysis of profilometer measurements (see section 3.2.5). For the first experiment, inductive coupled plasma etching with sulfur hexafluoride (SF_6) and O_2 was done for a number of samples with 10 nm-thick HZO thickness. Different time of etching is applied: 10 s, 30 s, and 60 s. After that, each one of these sample is cut into to two parts: one cleaned with acetone to remove photoresist, and the other left uncleaned for comparative analysis.

Profilometer measurements were then performed for all etched samples. the aim from these measurements is to measure the shape of profile line, or in other words measuring thickness amount of etched layer. In addition, from profilometer measurements, it was possible to check the thickness of photoresist for not etched sample. It was observed that photoresist is etched faster than W when the etching process is done by (SF_6 and O_2), although the photoresist is much thicker than the W.

Therefore, for the second experiment, ICP-etching with only SF_6 was decided. Hence, first experiment was repeated with SF_6 as etchant material for other samples of 10 nm HZO thickness. Profilometer measurement showed that thickness of etched layers is around 200 nm when time of etching is 25 s, which mean 150 nm W is totally removed and the etching is stopped approximately in SiO_2 layer. From here, the time of etching is selected to be 25 seconds for all the studied 3D HZO samples. Figure 3.8 displays schematic representation of the structure before and after etching, respectively.

3.1.5 Photoresist Stripping

Lift off process was performed for the samples to remove photoresist before RTA to prepare the samples for electrical and structural characterization. Firstly, the samples were cleaned by acetone in ultrasonic bath (US) at room temperature for 10 min then the samples

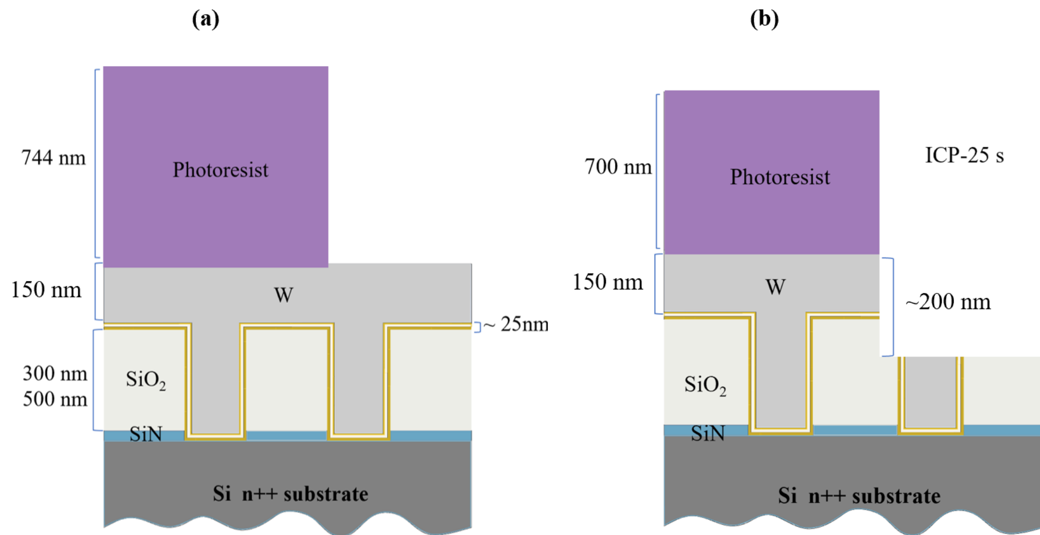

Figure 3.8: 2D Structure scheme of the samples. (a) Before ICP (b) After ICP etching.

were rinsed in isopropanol. Figure 3.9 displays the chemical bench where the samples cleaned in US bath. In the figure, the US plate, setting screen for US Bath and photo for cut samples are highlighted. After cleaning the samples by acetone in US path, high density radical flux (HDRF) stripping by oxygen plasma was employed to confirm that there is no residual photoresist before RTA. Stripping parameters by O_2 plasma include temperature of the substrate equal 90 °C, pressure equals 1800 mTorr, power of the plasma equals 2000 watts, and flow rate of oxygen equals 1000 sccm. The period time of HDRF stripping was 3 minutes for all the samples. Figure 3.10 displays HDRF stripper device located in BCAI clean room in CIME nanotech which was used for photoresist stripping of all studied samples.

3.1.6 Rapid Thermal Annealing

Rapid thermal annealing is widely used in semiconductor manufacturing to modify the structural properties of materials through short, high-temperature treatments. This technique enables precise control over material characteristics by rapidly heating the samples, minimizing thermal stress and defects (Sze, 2008). For semiconductor materials,

Figure 3.9: Chemical bench in BCAI clean room highlight samples prepared for stripping in US bath, US plate and setting screen for US cleaner.

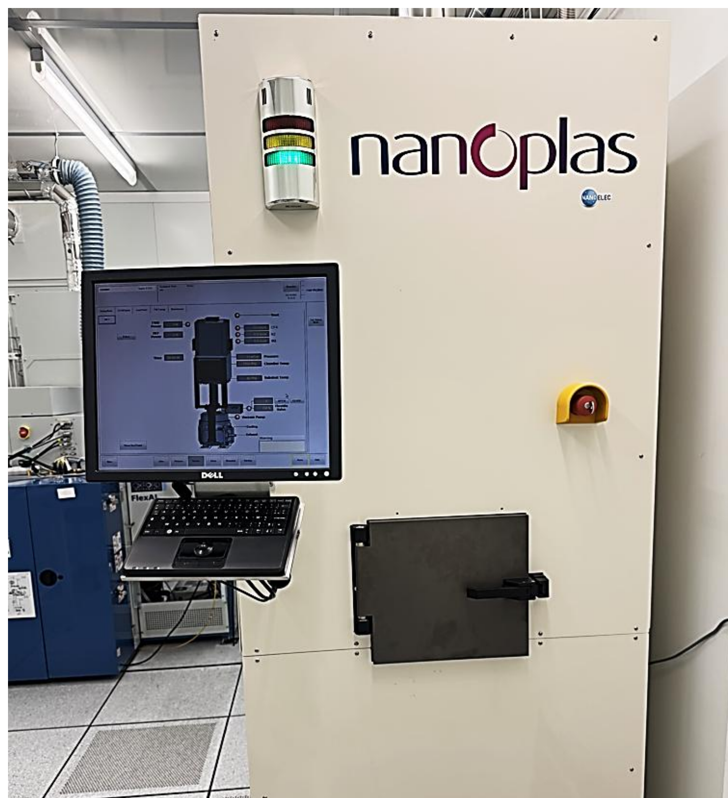

Figure 3.10: High density radical flux device used in O_2 plasma stripping.

RTA can improve the electrical and structural characteristics of thin films, enhances interface quality, and reduces defects, which are essential for high-performance devices (Plummer, 2009).

In this study, the annealing process was performed using the RTP-100 system from UniTemp GmbH, a front-loading rapid thermal vacuum process oven designed for precise temperature control. The temperature was increased at a rate of 25 °C/s until reaching the target annealing temperatures of 400 °C, 450 °C, and 500 °C. The samples were maintained at these temperatures for 10 minutes under a nitrogen (N_2) atmosphere to prevent oxidation and unwanted reactions (UniTemp GmbH). then quickly bringing it back to room temperature. Temperature regulation was achieved through thermocouples, ensuring uniform heating and controlled cooling.

Figure 3.11 displays cross section 3D scheme showing subsequent of the fabrication processes which ends with RTA annealing to prepare the samples for characterization. One group of samples with etched W was annealed for the electrical measurements, and another group of the same type of samples, but not-etched W layer was annealed for X-ray diffraction (XRD) measurements. Also, not annealed samples were prepared for both electrical and XRD measurements.

3.2 Structural and Physical Characterization

The structure of the prepared 3D TiN/HZO/TiN capacitor was characterized and analyzed by physical, structural characterization techniques. physical characterization which include X-ray reflection (XRR), scanning electron microscopy, optical image scanning and profilometer measurements were employed to examine surface morphology and structure dimensions to determine parameters needed in fabrication process and in electrical measurements. the structural characterization defined here by GIXRD measurements was employed for crystallographic analysis.

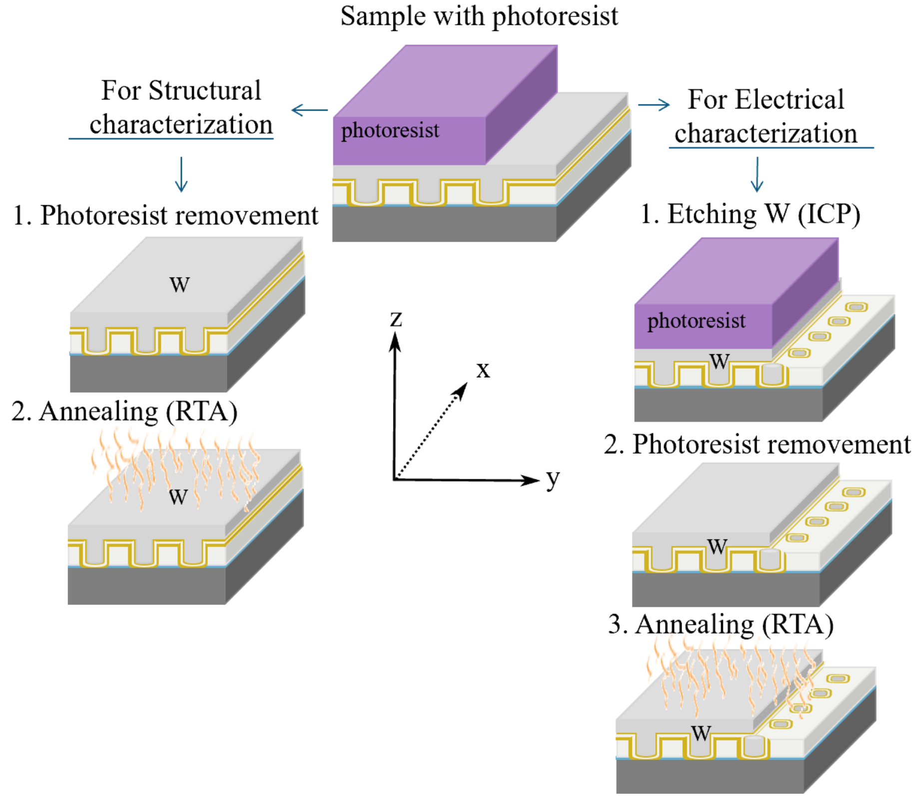

Figure 3.11: Fabrication process steps employed to prepare the samples for structural and electrical characterization.

3.2.1 X-ray Diffraction

X-ray diffraction is a non-destructive method used to examine the crystallographic structure, phase composition of thin films. It relies on the elastic scattering of incident X-ray photons by electrons in a material's atomic lattice (Pandey, 2021). When the conditions for constructive interference are met, diffracted beams produce a peak intensities that can be recorded as a function of incident angle, providing information on the orientations of atomic planes and interplanar spacing (Harrington, 2023). This is particularly important for evaluating the quality of thin ferroelectric films, such as HZO, where detecting phase transitions (e.g., monoclinic to orthorhombic) is essential.

In the present study, X-ray diffraction analyses were carried out using the grazing-incidence configuration to enhance the signal from the thin HZO layer while minimizing

substrate effects. The following subsection describes the GIXRD geometry, setup, and measurement parameters used.

3.2.1.1 Grazing Incidence X-ray Diffraction

The penetration depth of X-rays is in the 1–100 μm range, and because films are often substantially thinner, the substrate diffraction peak typically dominates the resultant pattern. The intensity of reflections from randomly-oriented polycrystalline films is often particularly low, as only a subset of the grains is contributing towards the signal. In GIXRD, the incidence angle, omega (ω), is fixed to a small angle of approximately 0.5–1°, slightly above the critical angle (below which total refection will occur), and the detector is moved on the 2θ-circle to collect the scattered wave in different angles as presented in Figure 3.12

In this way the penetration deeper into the sample is considerably reduced and the intensity of the film peaks is enhanced with respect that of substrate. The data obtained from GIXRD measurements provide valuable insights into the effects of the RTA process on the structural properties of the capacitors. By varying the incidence angle, it is possible to change the X-ray penetration depth. The incident angle which enabled enough penetration to HZO layer in the studied capacitor is 7°. This large value was needed due to the thick W layer which cover top electrode. The 2θ detection angle was varied in the range of 20°- 80°and in range of 27°- 34°.

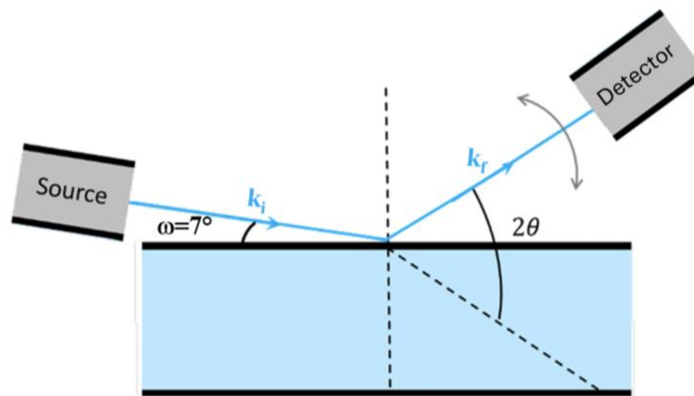

Figure 3.12: Diagram of the geometry used in GIXRD. $\mathbf{k}_i$ and $\mathbf{k}_f$ are the wave vectors of the incident and diffracted waves, respectively (Belahcen, 2022).

Grazing incident-XRD requires particular optics, with a parallel beam, very small incidence slit, and a parallel plate collimator in the diffracted beam. In this study, the crystallinity of the HZO layers was examined and analyzed by GIXRD using Empyrean, (Malvern Panalytical) diffractometer. The key parameters and setup for the GIXRD measurements are as follows:

- X-ray source: The measurements were conducted using a Cu K_α radiation source with a wavelength of 1.5406 Å.
- Incident beam path: The X-ray tube operated at 45 kV and 40 mA, with a line focus of 12 mm length and 0.4 mm width. The incident beam was conditioned using an parallel beam X-ray mirror for Cu radiation and Soller slits with an opening of 0.04 rad.
- Sample stage: The samples were mounted on a programmable x, y, z stage with minimum step sizes of 0.01 mm for X and Y axes, and 0.001 mm for the Z axis.
- Measurement Range: The GIXRD scans were performed in two ranges: 27° to 34° and 20° to 80° in 2θ, with a continuous scan mode. The common counting time was 20 seconds per step for the 27° to 34° range and 6 seconds per step for the 20° to 80° range. The step was 0.05° for (20°-80°) range and 0.02° for (27°-34°) range.
- Detector: A proportional detector filled with Xenon (Xe) gas was used to collect the diffracted X-rays, with a parallel plate collimator of 0.18° opening and a receiving slit height of 0.10 mm.

3.2.2 X-ray Reflectometry

X-ray reflectometry (XRR) is a nondestructive, surface-sensitive technique used to determine the thickness, roughness, and density of thin films. It operates by directing an X-ray beam at low angles toward the sample and measuring the intensity of the reflected beam as a function of the incident angle. When X-rays interact with a surface at grazing incidence, the reflection behavior depends on the angle relative to a material-specific threshold called the critical angle (θ_c). For incident angles below θ_c, total external reflection occurs, and the

X-ray beam does not penetrate the film. As the angle increases and exceeds θ_c, the beam enters the material, leading to a rapid decrease in reflected intensity. This transition reflects the interplay between reflection and refraction and depends on the film's composition and density (Yasaka, 2010).

In this study, XRR was employed to determine the critical angle θ_C of the HZO layers prior to conducting GIXRD measurements. The value of θ_C was extracted from the reflectivity curve by identifying the angular point at which the reflected intensity dropped to half of its maximum ($I_o/2$). This calibration step was essential for optimizing the incident angle used in GIXRD scans. Figure 3.13 illustrates the behavior of the reflected beam at different incident angles in relation to θ_C, showing the transition from total reflection to beam penetration.

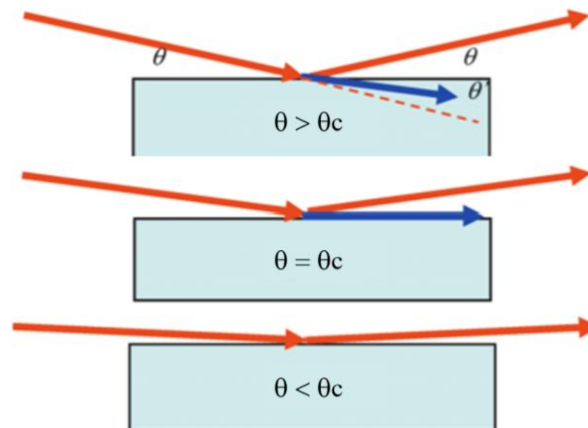

Figure 3.13: Reflection and refraction of X-rays at material surface with the changes in the grazing angle. Adapted from Yasaka (2010).

3.2.3 Scanning Electron Microscopy

Scanning electron microscopy is an imaging technique used to obtain high-resolution images of the surface morphology and provide topographical, compositional information about a wide range of materials. Scanning electron microscopy operates by directing a focused beam of high-energy electrons onto the surface of thin film. The interactions between the electrons and the sample produce various signals, such as secondary electrons,

backscattered electrons, and characteristic X-rays, which are detected to form detailed images and provide compositional information (Goldstein *et al*., 2017).

Scanning electron microscopy is extensively used in microelectronic researches, due to its high-resolution imaging, and its wide magnifications range (Reimer, 1998). In addition, SEM provides images with a greater depth of field, offering a 3D appearance to the images. In this study, Zeiss ULTRA Plus SEM equipped with the GEMINI column was used to scan the 3D HZO integrated capacitors. The device operates under high vacuum conditions to ensure optimal electron beam stability and imaging quality and has the following features:

- GEMINI optics: Providing high resolution and contrast for detailed surface characterization.
- Multiple detectors: Including secondary electron detector (SE_2) and InLens detector, allowing for versatile imaging modes.
- High-precision stage: Enabling accurate sample positioning with controls for X, Y, Z movement, tilt, and rotation.
- The SEM's control panel includes main components which are labeled in the right image of Figure 3.14. The components are:

    1) Dual monitors for real-time observation.
    2) Advanced control joysticks.
    3) Comprehensive keyboard interface for parameter adjustments.

In this work, SEM scanning was performed for three samples from top and cross section view. The three samples are not annealed and have same HZO thickness and same aspect ratio. The difference is in ICP etching time for them. Sample with longer etching time was scanned to obtain better vision for the 3D semi-cylindrical holes. The used detector are SE_2 and In Lens detectors with beam energy equal 5 kV and working distance around 5 mm.

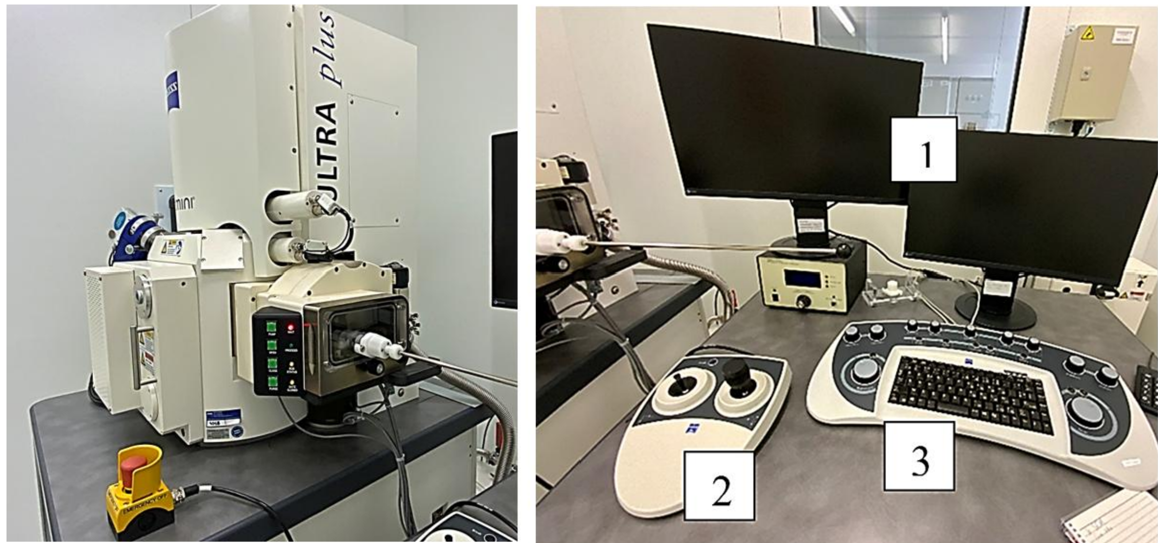

Figure 3.14: MEB Zeiss ULTRA Plus Scanning Electron Microscope device located at BCAI clean room in CIME.

3.2.4 Optical Microscope Scanning

During the fabrication process, specifically before and after each photoresist stripping and before RTA. It is important to check the surface of the samples and be sure that the photoresist is removed completely before RTA. For this porpose, optical microscope (Figure 3.15) was used to scan the surface of the the TiN/HZO/TiN samples. When the samples were stripped by acetone for two minutes, photoresist lines appeared in optical images of the stripped samples as can be seen in Figure 3.16 (a). It was predicted that this lines form residual photoresist and the devices are not totally clean.

To check that, optical images were taken for the samples after cleaning them by acetone in US bath for 10 minutes and for the samples after HDRF stripping with O_2 plasma for 3 minutes. The resulted images displayed in Figure 3.16 (c) showed disappearing the residual photoresist after acetone in US Bath for 10 minutes. In addition, the optical images displayed in Figure 3.16 (b) for the samples after O_2 plasma stripping displayed clean shiny devices with no residual photoresist.

Figure 3.15: Optical microscope located at BCAI clean room in CIME.

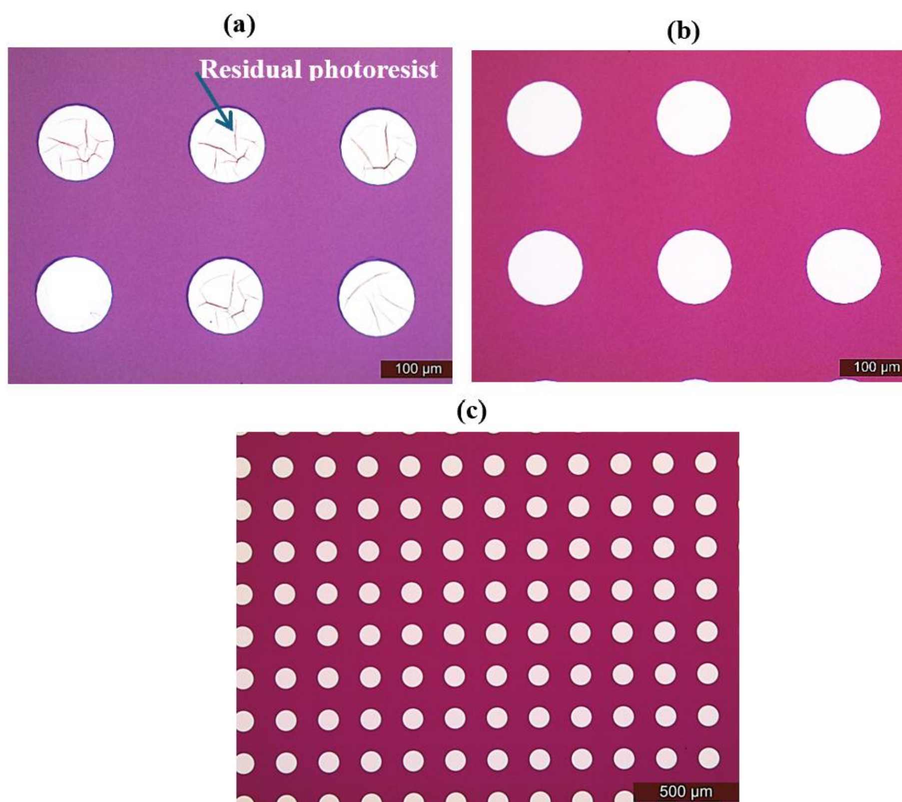

Figure 3.16: Optical images. (a) After cleaning with acetone for two minutes. (b) After O_2 plasma stripping for three minutes. (c) after cleaning with acetone in US path for 10 minutes.

3.2.5 Profilometer Measurements

Profilometer measurements are generally used for evaluating the surface topography, thickness, and roughness of devices (Lee *et al*., 2023). It plays a significant role in ensuring the quality and uniformity of thin films and patterned surfaces, which directly affects the performance of the final devices. In this study, it was used for determining some dimensions and parameters in addition to critical decisions and suggestions for the progress of the fabrication process particularly, for ICP etching and stripping treatments, Supporting development of reliable procedures for the study.

The profilometer operates by tracing the surface of the sample with a high-precision stylus (sharp contacting prob) that moves laterally across the surface. As the stylus traverses peaks and valleys, it records the vertical displacement, providing detailed information about the surface profile. Key parameters were recorded during these measurements include the scan length, scan resolution, stylus force, and scan duration, which collectively influence the accuracy and resolution of the data (Pomberger et al., 2019). Figure 3.17 displays the equipment used for the profile measurements of the studied samples.

Figure 3.17: DektakXT Stylus Profiler at BCAI clean room in CIME.

As mentioned in section 3.1.4 (p.42), etching time was selected after analysis of profilometer measurements for samples etched with different time. In addition, profilometer measurements confirmed that the apparent lines after acetone for only 2 minutes, refers to residual photoresist. Such that when stylus move on one line, sharp peak appear in the curve of profile hight. The profilometer settings included a scan length of 2 mm, a scan duration of 10 seconds, and a stylus force of 3 mg (≈ 29.4 µN). The stylus, with a radius of 12.5 µm, ensured precise contact with the surface, capturing detailed height variations across the sample.

Figure 3.18 provides the surface profiles for sample with lines on surface of its contacts (Figure 3.18 (a)), and for sample without this lines on surface of its contacts (Figure 3.18 (b)). The data reveals notable differences in surface roughness and thickness, indicating the effectiveness of the stripping process.

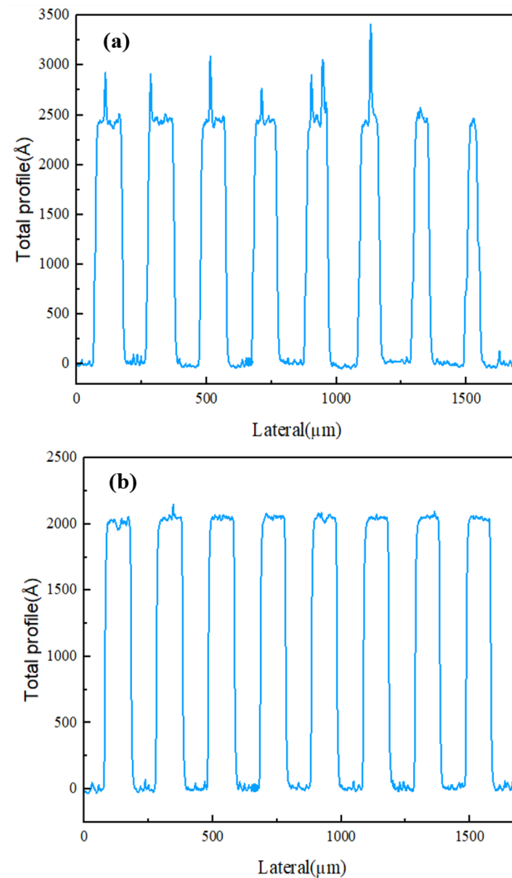

Figure 3.18: Profile measurements for samples with (a) residual photoresist. (b) no residual photoresist.

3.3 Electrical Characterization

The electrical properties of the samples form the basic features that reveal the ferroelectric behavior. Largest part of the results in this study is referred to the electrical characterization, which examine the performance and reliability of the devices. After the physical and structural investigation, the samples were subjected to several electrical tests to measure the parameters needed in electronic devices. The electrical tests included: leakage current (I-V), capacitance-voltage (C-V), polarization-electric field, Dynamic hysteresis measurements (DHM) and endurance measurements. These measurements allow to extract some parameters of ferroelectric: the coercive field, remanent polarization cycling behavior, and leakage current density.

All the electrical tests were done using a manual probe station, which make electrical contacts with the samples. The probe station had micromanipulator probes to place them precisely on the electrodes of the samples. The top probe on the top electrode (W), While the bottom electrode (Si++ substrate; back surface of the sample) on a metallic plate connected directly by a cable to the bottom probe. Figure 3.19 displays HZO sample under test with the electrical probes on the top and bottom electrodes.

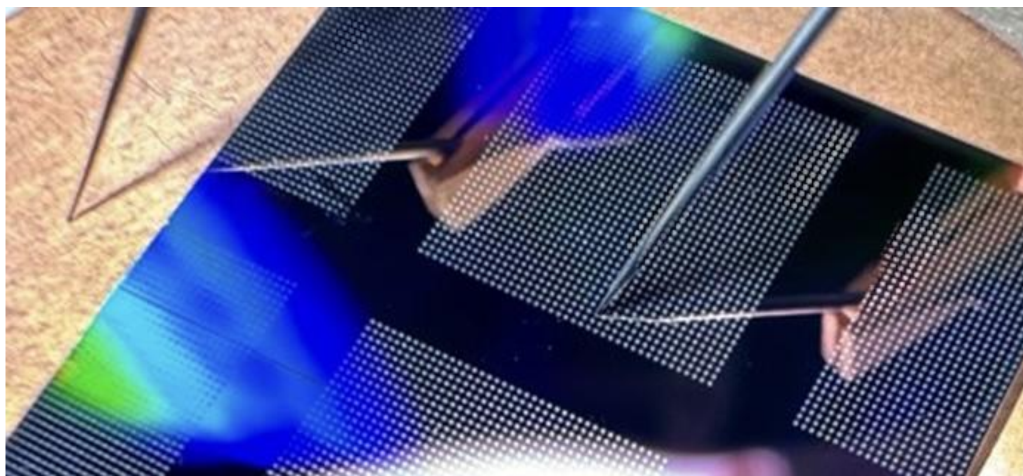

Figure 3.19: HZO sample under test, with the electrical probes on the top and bottom electrodes.

3.3.1 Leakage Current Measurements

Leakage current measurement was used for evaluating the conductivity of the electronic devices. Since leakage current affects the overall performance and reliability of the devices, it is fundamental to measure and minimize it for most technological applications. High leakage currents can lead to early electrical breakdown, degrading the quality and functionality of capacitors and other electronic components.

In the present study, I-V characteristics were measured by a probe station setup (Figure 3.20 (a)) and a Source Monitor Unit (SMU) using a Keithley-2612B-dual-channel system (Figure 3.20 (b)). Two conductive probes were placed in contact with the top and bottom electrodes of the capacitor. The top probe was placed to make a contact with the W metallic layer, acting as the top electrode, while the bottom probe was positioned to connect with the TiN electrode from the back surface of the samples through the highly doped Si_{n++} substrate.

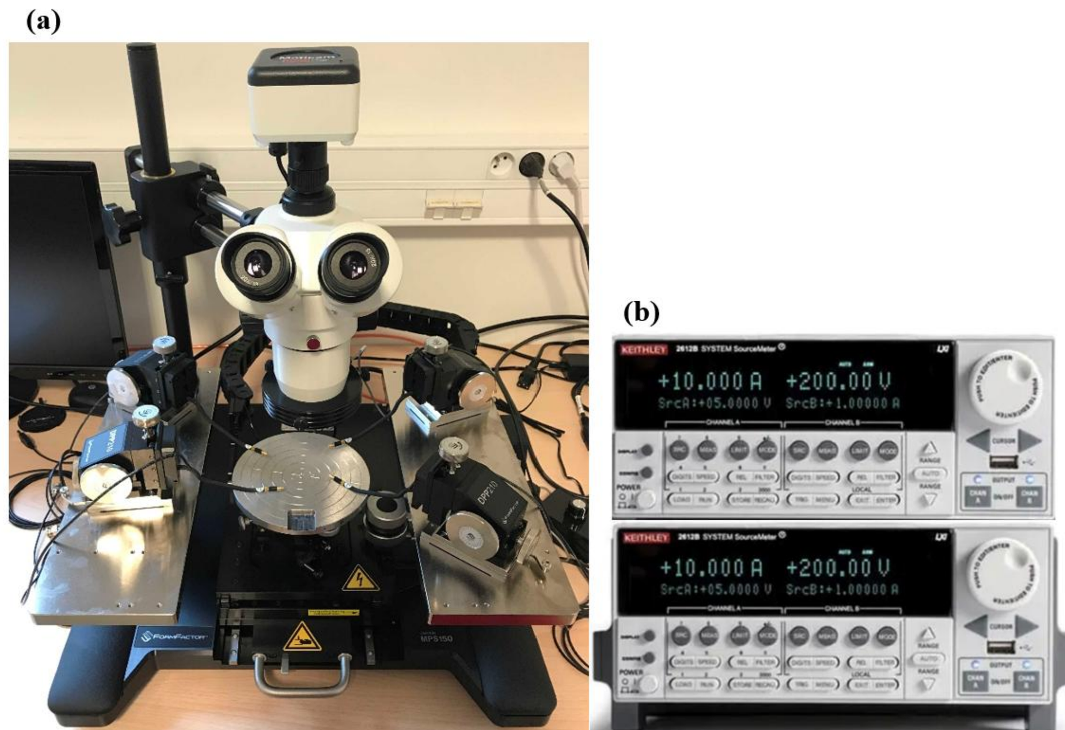

Figure 3.20: (a) probe station used to connect the electrodes of the device. (b) Keithley-2612B-dual-channel system.

The SMU is operated in voltage-mode by a software (automated characterization suite (ACS)) that produce the data; voltage sweep according to the test recipe along with current's results. The measurement is performed under a DC applied bias to analyze the I-V characteristics. An externally applied voltage induced a leakage current through the ferroelectric material, which depended on the mobility of free electronic or ionic charges in the dielectric properties. High leakage currents could interfere with the material's ferroelectric properties, affecting its stability and long-term performance.

3.3.2 Capacitance-Voltage Measurements

The ferroelectric behavior of the MFM capacitor can be observed through the capacitance-voltage characteristics, which exhibit a distinctive butterfly-shaped curve. The C-V characteristic provides a rapid and straightforward method for detecting ferroelectric properties, making it an ideal initial approach for this study. This is the primary reason for its use in this thesis. To measure the MFM capacitance, a small alternating current (AC) signal is superimposed on a direct current (DC) bias. Using an LCR meter, capacitance is measured at each DC voltage step, with the AC signal of constant amplitude and frequency.

Ferroelectrics display a nonlinear C-V response due to polarization switching that occurs when the coercive voltage is approached and this leads to significant capacitance increase. This occurs twice in ferroelectric materials, creating a butterfly-shaped loop. The AC signal frequency and amplitude are typically ranging from 1 kHz to 100 kHz, and ~ 50 mV, respectively.

Figure 3.21 illustrates the C-V measurement principle. A small AC signal is applied over a stepped DC voltage, allowing the capacitance to be measured as a function of bias. The resulting C-V curve is then integrated to extract the corresponding charge-voltage which is useful for analyzing ferroelectric polarization. This approach helps highlighting the nonlinear response characteristic of ferroelectric materials.

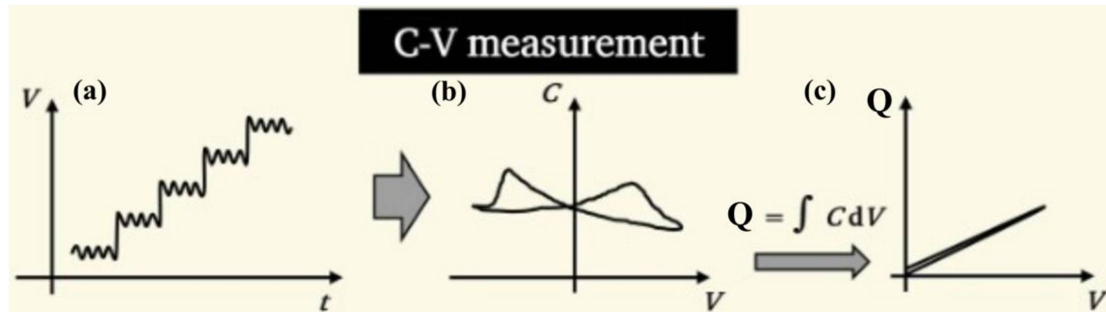

Figure 3.21: Schematic representation of the C-V measurement process. (a) A stepwise DC bias is applied along with a small AC signal . (b)The capacitance response is recorded over the voltage sweep, forming a butterfly-shaped C-V curve. (c) Integration of the capacitance yields the total charge (Zagni et al., 2023).

3.3.3 Polarization Field Measurements

Polarization field measurements (PM) are fundamental in evaluating the ferroelectric properties of materials, providing insights into their switching behavior and charge retention capabilities (Stewart, 1999). One typical measurement is the very common PUND pulse sequence with two positive and two negative consecutive pulses. It is used for measuring the remanent polarization of ferroelectric capacitors. It allows to distinguish the true polarization response from non-ferroelectric contributions such as leakage currents or capacitive effects (Martin, 2016).

The PUND technique involves applying a sequence of voltage pulses to the device under test and recording the resulting current response. The pulse sequence consists of two positive and two negative pulses applied consecutively as depicted in Figure 3.22. The first positive and negative pulses allow the ferroelectric domains to fully switch, while the second pair measures the real remanent polarization without contributions from transient or leakage currents (Scott, 1988). In comparison to the DHM, the PM uses unipolar rectangular pulses. The rise time of these pulses is adjustable.

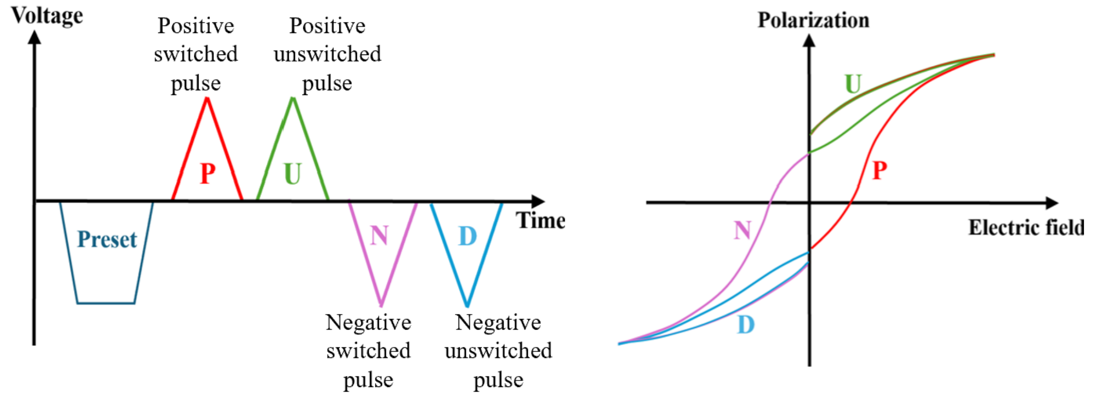

Figure 3.22: Schematic of PUND measurements.

In this study, Thin film 300 analyzer from Aixact system with prob station setup (Figure 3.23) was used for PUND testing, with triangle mode for pulse train. The applied pulse parameters, including voltage amplitude, pulse width, delay time and rise time, were carefully adjusted. Voltage amplitude was adjusted depending on the value of electric field. Rise time forms basic parameter which determine PUND frequency. PUND frequency was fixed at 10 kHz (rise time ~25µs). pulse width was adjusted to the same value of rise time, delay time which revealed better results at 1s was set at 1s, finally, current range take value of 1mA when PUND frequency is 10 kHz. On the other hand, the extracted data was processed intensively using Python program to plot hysteresis loops, providing a clear visualization of the ferroelectric switching behavior.

Additionally, Dynamic Hysteresis Measurement (DHM) were conducted to further analyze polarization characteristics under varying conditions. These measurements complement the PUND technique by offering a broader understanding of domain dynamics and charge retention over multiple cycles. The DHM records the hysteresis loop of a ferroelectric material and assists to examine the influence of process parameters on the shape of the hysteresis loop. Measurement parameters like amplitude, frequency and delay time of the excitation signal can be varied. The wave signal is displayed in Figure 3.24 and shows DHM setup parameters. The software of Aixact extracts the characteristic values like P_r, V_c from the hysteresis loop.

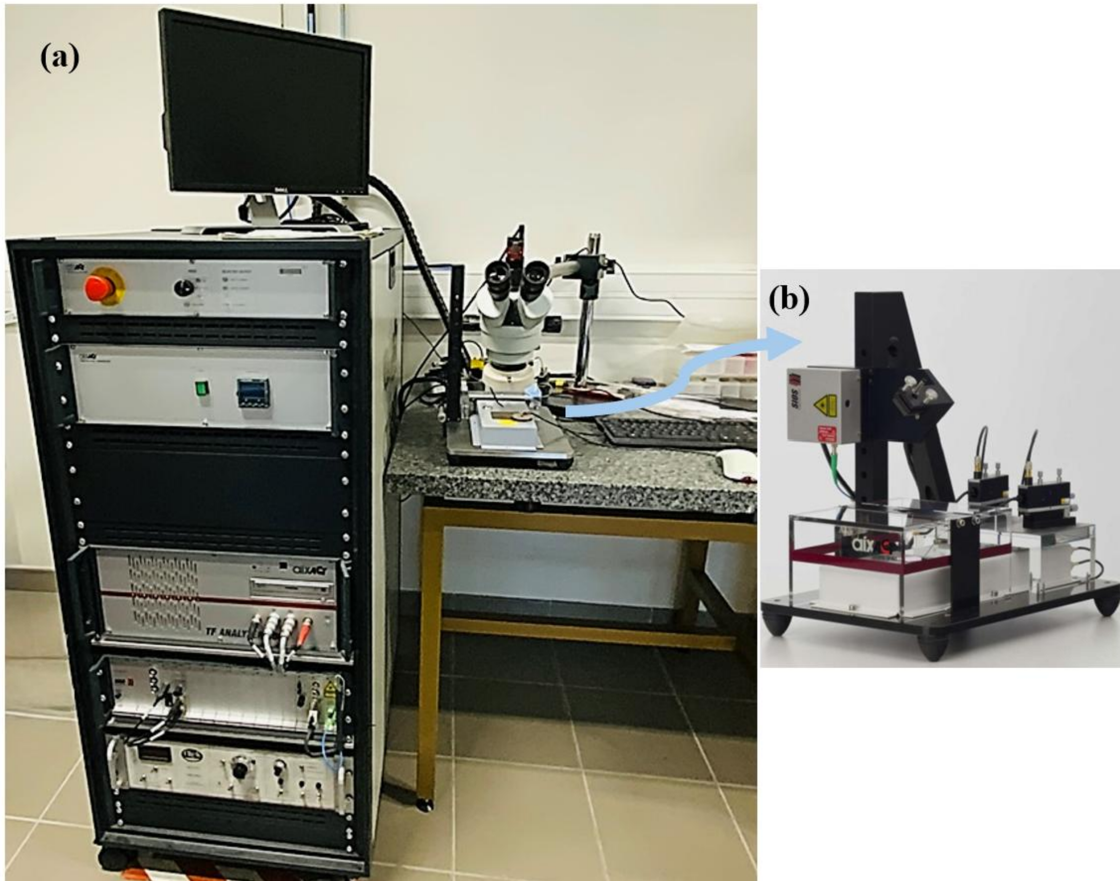

Figure 3.23: (a) Aixact TF 300 analyzer used in electronic lab in CIME. (b) The prob station from Aixact.

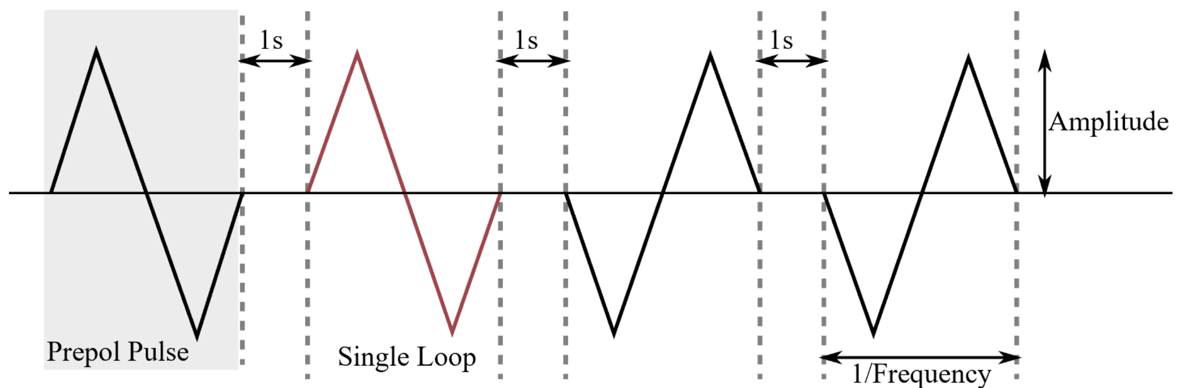

Figure 3.24: Triangular wave signal for DHM setup parameters.

3.3.4 Endurance Measurements

Endurance measurements, also referred to as fatigue measurements (FM) in the Aixact system, were conducted to evaluate the reliability and endurance of the ferroelectric samples under repeated electrical stress. It is used for understanding how ferroelectric properties evolve with cycling. In this study, endurance tests were performed at two different cycling frequencies: 1 kHz and 100 kHz, with each frequency tested at two different electric field amplitude, 3 MV/cm and 4 MV/cm. This approach enabled a detailed investigation of the impact of both cycling frequency and electric field on the endurance characteristics of the samples.

The PUND pulse train was applied at 10 kHz throughout the measurements to track polarization behavior systematically. The measurement protocol consisted of alternating between cycling and PUND pulses, as illustrated in Figure 3.25. During the cycling phase, the samples were subjected to repeated square voltage pulses, which served as write pulses to continuously switch the polarization state and simulate device operation over time. These square pulses were not used for measurement but for stressing the ferroelectric layers through cyclic polarization reversal.

In contrast, the triangular PUND waveform constituted the read pulses, which were applied periodically to extract the polarization–electric field hysteresis loops. This PUND method enables accurate evaluation of the switchable and non-switchable components of polarization, thereby allowing assessment of ferroelectric degradation during cycling. Figure 3.25 also highlights the rise time of the triangular PUND pulses. To achieve a PUND frequency of 10 kHz, the rise time was set to 25 μs.

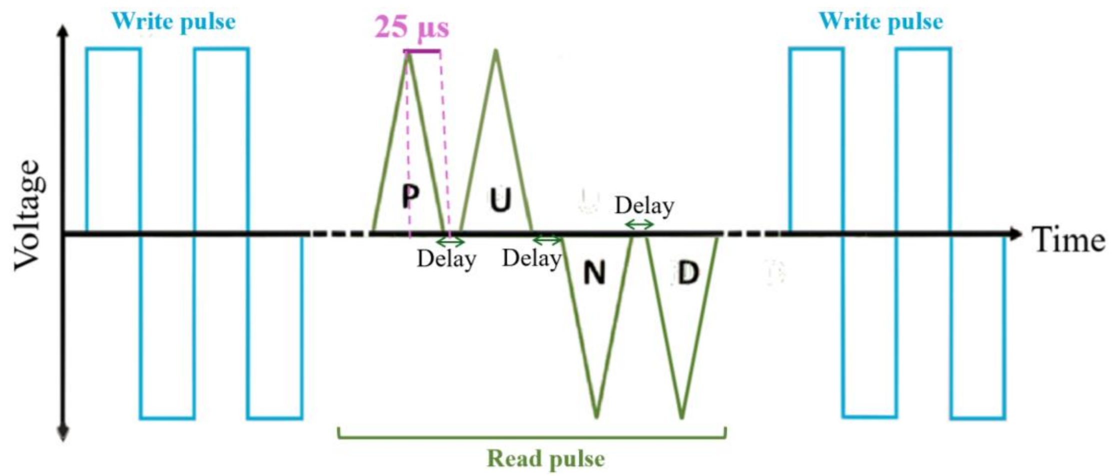

Figure 3.25: Pulse train used during endurance measurements, consisting of alternating square wave pulses (write pulses) for continuous cycling and triangular PUND pulses (read pulses) for electrical characterization.

Chapter Four: Results

This chapter presents the results of the experimental work carried out on the 3D TiN/HZO/TiN capacitors. The findings are organized into three parts: physical, structural, and electrical results. The results reflect how the devices respond to changes in key parameters such as HZO thickness, annealing temperature, aspect ratio, and electric field value. In the “physical results” section, SEM is used to examine the geometry of the fabricated devices.The structural section focuses on GIXRD analysis to explore the crystallinity of the HZO layer and the formation of the orthorhombic ferroelectric phase. The electrical section presents measurements including C–V curves, leakage tests, DHM, PUND, and endurance testing, which helps to evaluate the switching behavior and reliability of the devices.

4.1 Physical Results Analysis

The physical properties of the developed capacitor structures are highlighted in this section. Scanning electron microscopy is used for geometrical investigation. Throughout the fabrication process, SEM was employed to verify the devices' geometry and to determine the main dimensions of the structure, to find surface area of the capacitors.

4.1.1 Scanning Electron Microscopy Images

The geometry of the 3D HZO integrated capacitor, described previously in Section 3.1, was investigated and confirmed using scanning electron microscopy. SEM measurements were performed on three non-annealed samples with an HZO thickness of 10 nm and an aspect ratio of 300/300. Figure 4.1 displays SEM images of the sample etched with the selected ICP etching time of 25 s after photoresist removal. The measurements were performed using an SE_2 detector with beam energy of 5 kV and a working distance of 5.4 mm. Figure 4.1 (a) shows a top-view image at 758X magnification, revealing

rounded polygonal tungsten contacts with a diameter of 100 µm. Figure 4.1 (b) presents the same device at higher magnification (6.59 kX), where the semi-cylindrical holes forming the 3D capacitor structure are clearly visible.

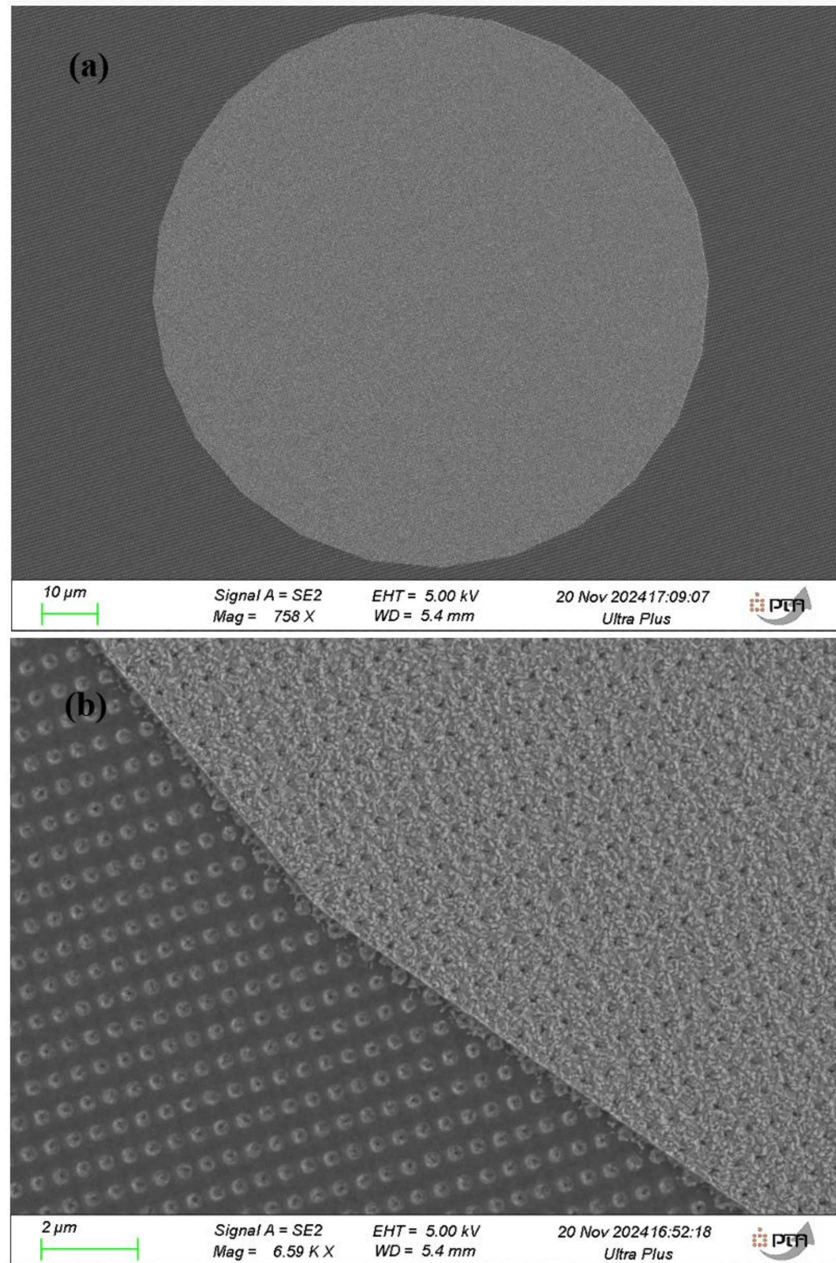

Figure 4.1: Top-view SEM images of the sample etched for 25 s (a) 758 X magnification. (b) 6.59 KX magnification.

To obtain a clearer view of the 3D hole structure, additional SEM imaging was performed on samples etched for longer time. Figure 4.2 shows top-view images of a sample

with an ICP etching time of 60 s. The low-magnification image (Figure 4.2 (a), 83X) reveals the array of circular W top electrodes defining the MFM capacitors with a fixed diameter of 100 µm. The higher-magnification image (Figure 4.2 (b), 11.23kX) resolves the semi-cylindrical holes that form the 3D structure. The zoomed-in region on the right side of Figure 4.2 (b) shows the geometric dimensions used for determining the capacitor surface-area. The pitch between holes is 364 nm in the y direction and 215 nm in the x direction, while the hole width is approximately 280 nm.

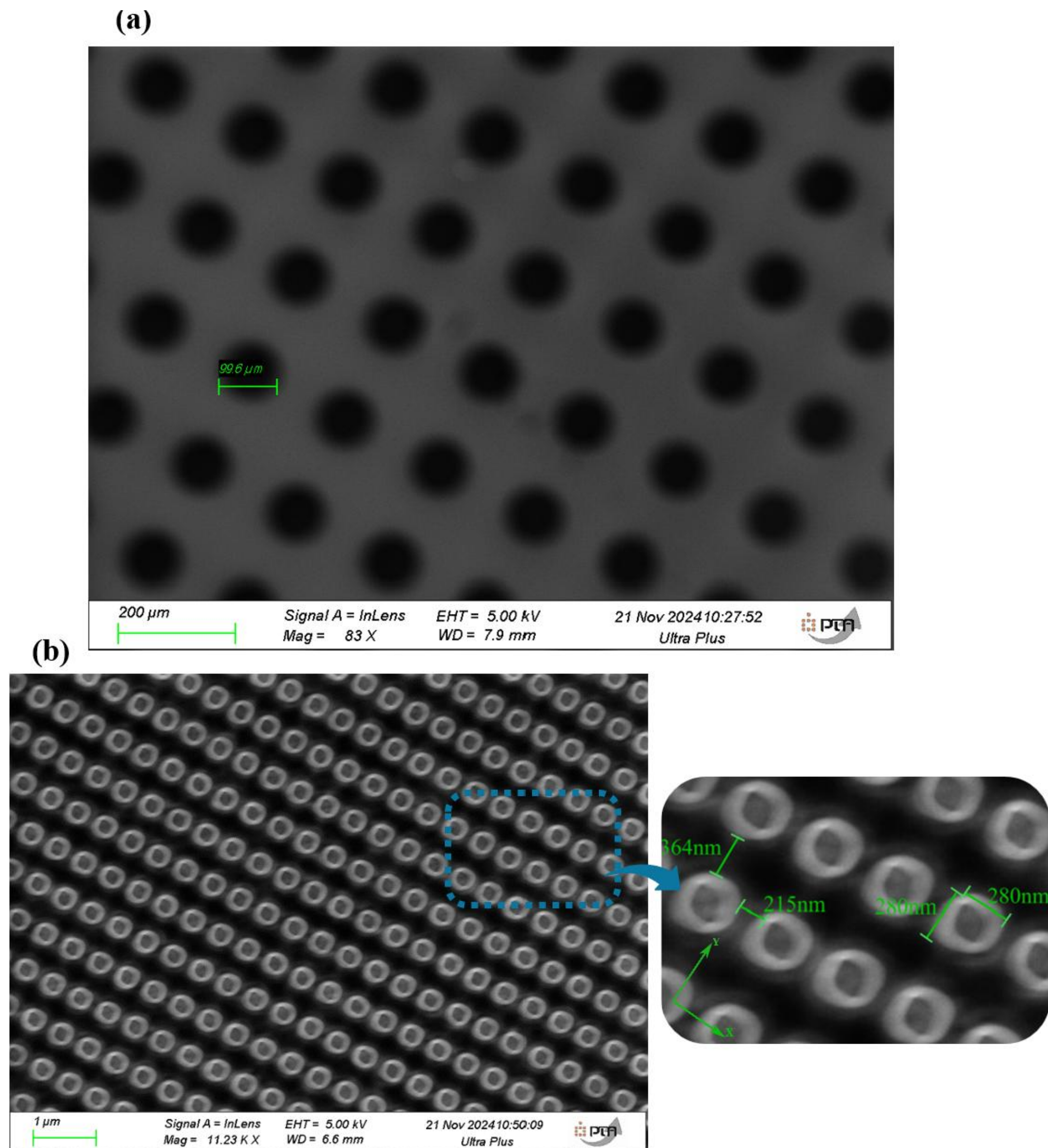

Figure 4.2: Top view SEM images of the sample etched for 60 s. (a) 83X magnification. (b) 11.23 KX magnification (left); zoomed-in image with hole dimensions (right).

Scanning electron microscopy imaging was also performed on cross-sectional samples. Figure 4.3 shows a cross-sectional SEM image of a sample etched for 25 s (AR 300/300). The image reveals the silver-colored tungsten layer (~150 nm thick) covering the surface and filling the holes of the 3D structure. The SiO_2 layer below has an estimated height of ~300 nm. The distance between adjacent holes appears to be ~400 nm, consistent with the pitch measured from Figure 4.2 (b) (364 nm). The observed hole width of ~300 nm is also in close agreement with the measured value of 280 nm.

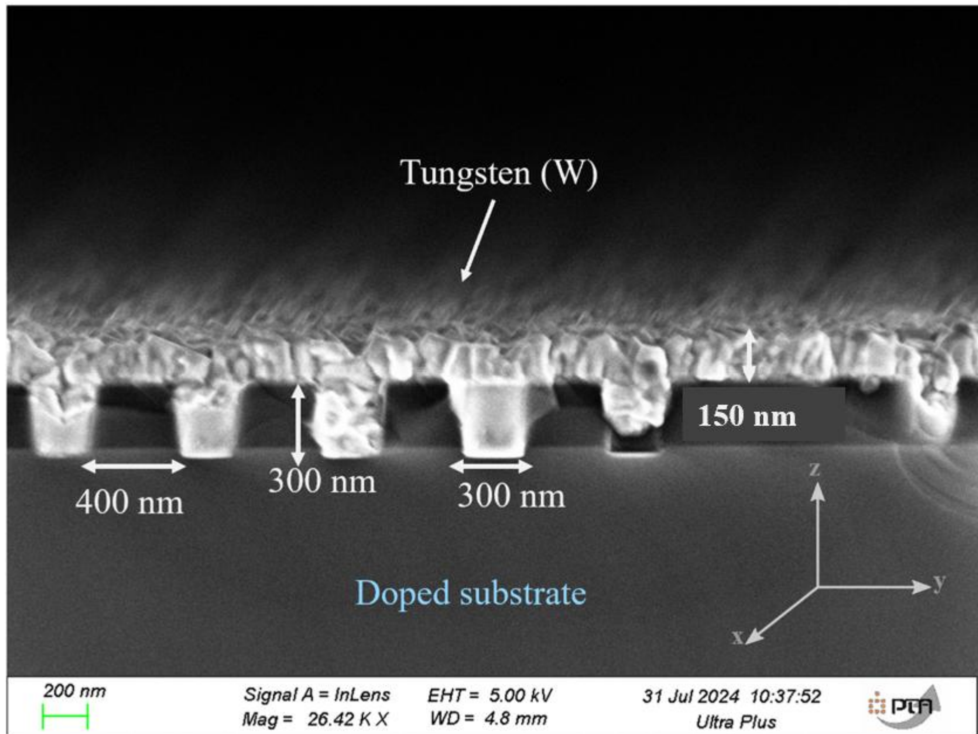

Figure 4.3: Cross-sectional SEM image for sample etched for 25 s (AR $_{300/300}$).

The geometric dimensions obtained from SEM imaging were used to calculate the total surface area of the 3D capacitors. These calculations enable comparison between 3D and planar (2D) surface areas and are later used in the electrical analysis to correct the remanent polarization values. Figure 4.4 presents a schematic illustration of the holes structure, indicating the lateral and planar surface components. Based on the dimensions obtained from Figure 4.2 (b), and Figure 4.3 , the parameters in Figure 4.4 can be defined as:

$a = (215 + 280)$ nm, $\quad b = (364 + 280)$ nm, $\quad d = 275$ nm,

$$h = \begin{cases} 500 \text{ nm}, & \text{for AR } 500/300 \\ 300 \text{ nm}, & \text{for AR } 300/300 \end{cases}$$

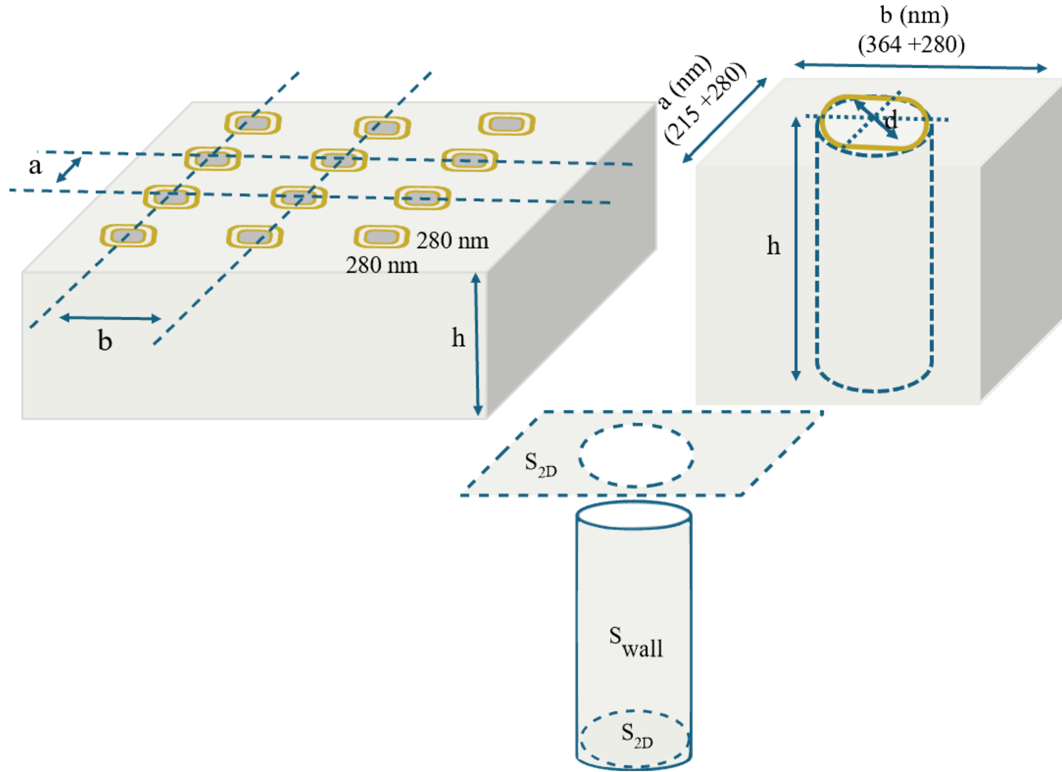

Figure 4.4: Schematic representation of the devices showing the surface area of one hole (Lateral surface (S_{wall}), Top and bottom 2D surface)).

The total 3D surface area S_{3D} for one hole can be expressed as:

$$S_{3D} = S_{2D} + S_{wall} \tag{4.1}$$

where

$$S_{2D} = a.b = 318780 \, nm^2 \tag{4.2}$$

and

$$S_{wall} = h.d.\pi \tag{4.3}$$

Substituting the measured dimensions gives:

$$S_{wall\left(AR_{\frac{500}{300}}\right)} = 431750\ nm^2$$

$$S_{wall\left(AR_{\frac{300}{300}}\right)} = 259050\ nm^2$$

Then

$$S_{3D}\left(AR_{\frac{500}{300}}\right) = S_{2D} + S_{wall}\left(AR_{\frac{500}{300}}\right) = 747326\ nm^2$$

$$S_{3D}\left(AR_{\frac{300}{300}}\right) = S_{2D} + S_{wall}\left(AR_{\frac{300}{300}}\right) = 574626\ \ nm^2$$

Accordingly, the ratios between the 3D and 2D surface areas are:

$$S_{3D}\left(AR_{\frac{500}{300}}\right)/S_{2D} = 2.34$$

$$S_{3D}\left(AR_{\frac{300}{300}}\right)/S_{2D} = 1.8$$

These calculated ratios represent the effective increase in surface area of the 3D capacitors compared to their 2D counterparts. They quantifies how much additional active surface is available for charge storage due to the presence of semi-cylindrical sidewalls in the 3D geometry. In addition, they are employed in the electrical analysis to correct the experimentally obtained polarization values for the actual 3D surface area.

To determine the total surface area of the capacitors, these ratios should be multiplied with the 2D total area, which corresponds to the area of the top circular W electrode with a diameter of 100 µm (Figure 4.1(a)), the total capacitor surface areas are:

$$S_{2D(total)} = \pi r^2 = 7850\ \mu m^2$$

$$S_{3D(total)}\left(AR_{\frac{300}{300}}\right) = 7850\ X1.8 = 14130 \mu m^2 = 1.413X10^{-8}m^2$$

$$S_{3D(total)}\left(AR_{\frac{500}{300}}\right) = 7850\ X2.34 = 18369 \mu m^2 = 1.837\mathrm{X}10^{-8}m^2$$

To evaluate the significance of the aspect ratio parameter, the ratio between the total surface areas of the two aspect-ratio designs is determined:

$$\frac{S_{3D}\left(AR_{\frac{500}{300}}\right)}{S_{3D}\left(AR_{\frac{300}{300}}\right)} = \frac{7850\text{x } 2.34}{7850\text{x } 1.8} = 1.3$$

This indicates that the capacitor with the higher aspect ratio (500/300) possesses a ~30% larger effective surface area compared with the lower-aspect-ratio design (300/300). In electrical analysis, this value is obtained in most of results analysis when comparing between the two different aspect ratio samples. confirming the good agreement between structural and electrical measurements.

4.2 Structural Results Analysis

The crystallographic investigation of the HZO layer using GIXRD is the main topic of this section. The measurements are intended to evaluate the effects of process parameters on the phase development and crystallinity of the ferroelectric layer, including incidence angle, annealing temperature, aspect ratio, and HZO thickness.

4.2.1 X-ray Reflectometry Measurement

Before performing GIXRD measurements, an X-ray reflectivity scan was carried out to determine the critical angle α_c for the studied 3D TiN/HZO/TiN structure. Figure 4.5 shows the intensity of the reflected X-rays as a function of the incident angle (α), in the low angle range from 0.1° to 0.9°. As seen in the figure, the reflected intensity is initially very high at small incident angles and then drops sharply around $\alpha \approx 0.3°$. This sudden decrease corresponds to the critical angle, beyond which the X-rays begin to penetrate the film rather than reflect entirely from the surface.

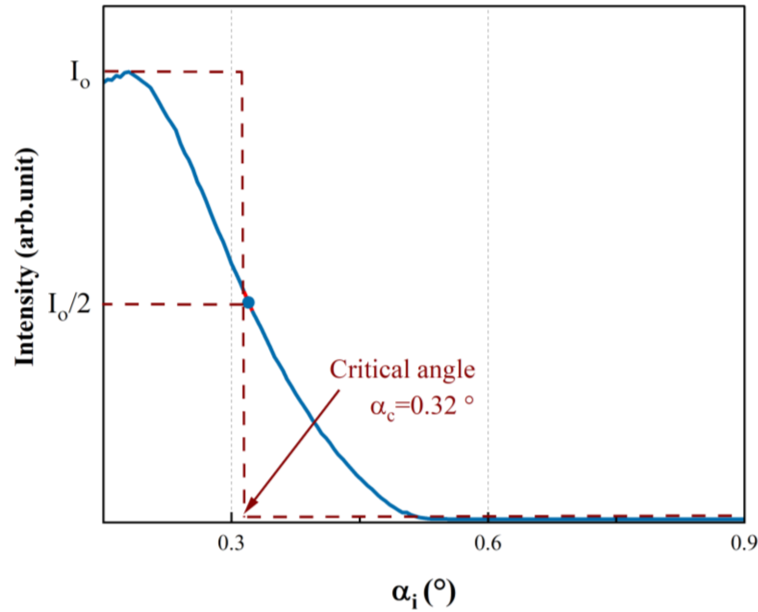

Figure 4.5: X-ray reflectivity measurement for critical Angle determination.

This behavior is typical of thin-film structures with dense materials like tungsten and HZO. Identifying the critical angle was an important step for selecting the appropriate incidence angle range for GIXRD analysis. Operating slightly above this angle allows the X-ray beam to interact effectively with the thin HZO layer while still limiting the contribution from the underlying substrate.

4.2.2 Incidence Angle Determination

After determining the critical incident angle at which the X-ray beam starts to penetrate layers of the studied samples, which are covered by a thick W layer (about 150nm), during first performed GIXRD measurements, it was observed that X-ray beam doesn't penetrate HZO layer when the incident angles omega (ω) is small. The peaks in the obtained XRD spectra correspond to the W layer and the detectable signals from HZO layer are very small.

Therefore it was necessary to choose a high enough ω angle, to penetrate deeper and to detect XRD signals from HZO layer. Thus, for two samples with HZO thickness 10nm

annealed at 500 °C with different aspect ratios 500/300 and 300/300, 2θ-scans were measured at different fixed ω angles. Figure 4.6 displays results of an experiment performed to test different values of incident angles ω.

Figure 4.6 (a) and Figure 4.6 (b) present the 2θ-scans obtained from the samples with aspect ratios of 500/300 and 300/300, respectively, for a series of fixed incident angles (ω = 1°–14°). The scans were recorded within the 2θ range of [27–34]°, although the displayed region in the figures is narrower. In this angular window, the main diffraction peaks corresponding to the monoclinic, tetragonal, and orthorhombic phases of crystalline HZO are expected.

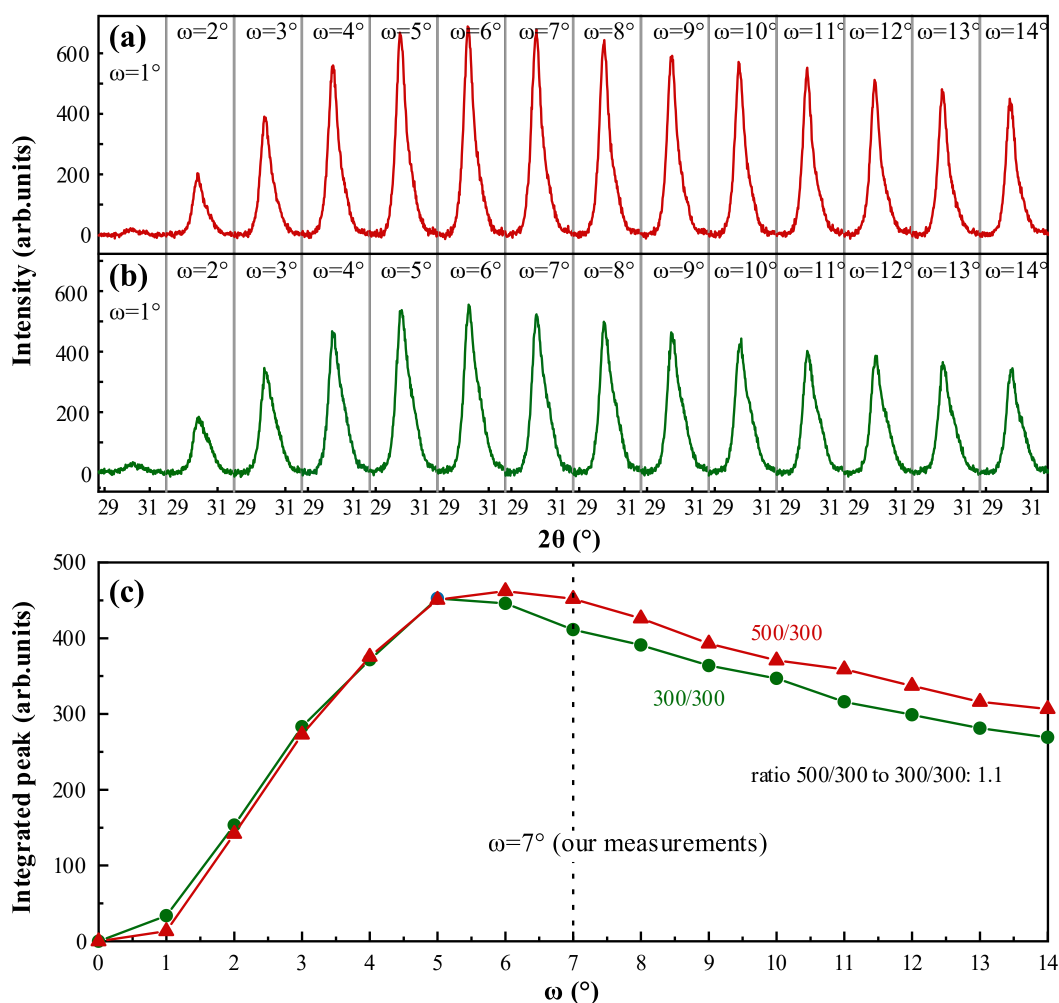

Figure 4.6 : XRD measurements at different incident angle ω for samples of 10 nm thick HZO (annealed at 500◦C) with an Aspect ratio (a) 500/300 and (b) 300/300. (c) Integrated peak intensity as a function of ω.

For both aspect ratios, the diffracted intensity rises as ω increases from 1° to about 5°. A plateau region follows, where the peak intensity remains nearly unchanged within ω = 5–7° for the 500/300 sample and ω = 5–6° for the 300/300 sample. Beyond these ranges, the diffraction peaks gradually weaken with increasing incident angle, i.e., for ω = 8–14° in the 500/300 case and ω = 7–14° in the 300/300 case. The reduction in peak height at higher ω values is associated with the smaller beam footprint and, consequently, a reduced interaction volume between the X-ray beam and the sample surface.

To choose the incident angle ω for all of these XRD measurements, integrated XRD peak intensity was plotted as a function of ω angle. XRD peak intensities, measured for 2 samples with different aspect ratios, were integrated in the 2θ range [27-34]°. Figure 4.6 (c) shows integrated peak intensity as a function of ω for this two samples. For higher ω and more HZO is probed, Beyond this ω range, the intensity gradually decreases. (beam footprint on the sample decreases reducing the measurement area).

Other observation is that in the ω angle range [7-14]°, integrated peak intensities for the samples with measured HZO surface $S_{3D\ 500/300}$ is always higher than for ones measured for HZO surface $S_{3D\ 300/300}$. This difference between measured integrated intensities for these two samples is due to the difference in HZO surface areas (more HZO for the $S_{3D\ 500/300}$ compared to the $S_{3D\ 300/300}$). This behavior is expected because a larger surface area increases the volume of material interacting with the beam and more photons being diffracted in the X-ray beam.

As a result of these measurements, the incident ω-angle was selected to be 7° for all XRD scans for all samples. The choice of ω equal 7° was made because at this value, X-ray beam sufficiently penetrates the HZO layer while maintaining a strong diffraction signal. At ω = 7°, the integrated intensity is close to its maximum value, as shown in Figure 4.6 (c), while avoiding the rapid drop in intensity observed beyond this angle due to the diminishing beam footprint. In addition, selecting ω = 7° provides greater stability and reproducibility. While the maximum intensity may occur closer to 6°, the signal in this region is highly sensitive to small misalignments, leading to noticeable variations. At 7°, the diffracted intensity is still near its maximum but remains relatively stable over a broader

range, making it less error-prone and more reliable for comparison between samples with slightly different optimal angles.

4.2.3 Grazing Incident X-ray Diffraction Spectra

To study the crystallographic properties of the films, GIXRD measurements with incident angle equal 7° were performed in the 2θ range of 20°–80° for all the samples. As shown in Figure 4.7 and Figure 4.8, the diffraction spectra reveal that the main peaks originate from cubic tungsten (W), which were identified by comparison with the standard PDF cards 00-047-1319 and 04-004-0806 corresponding to the space groups Pm-3n (223) and Im-3m (229), respectively.

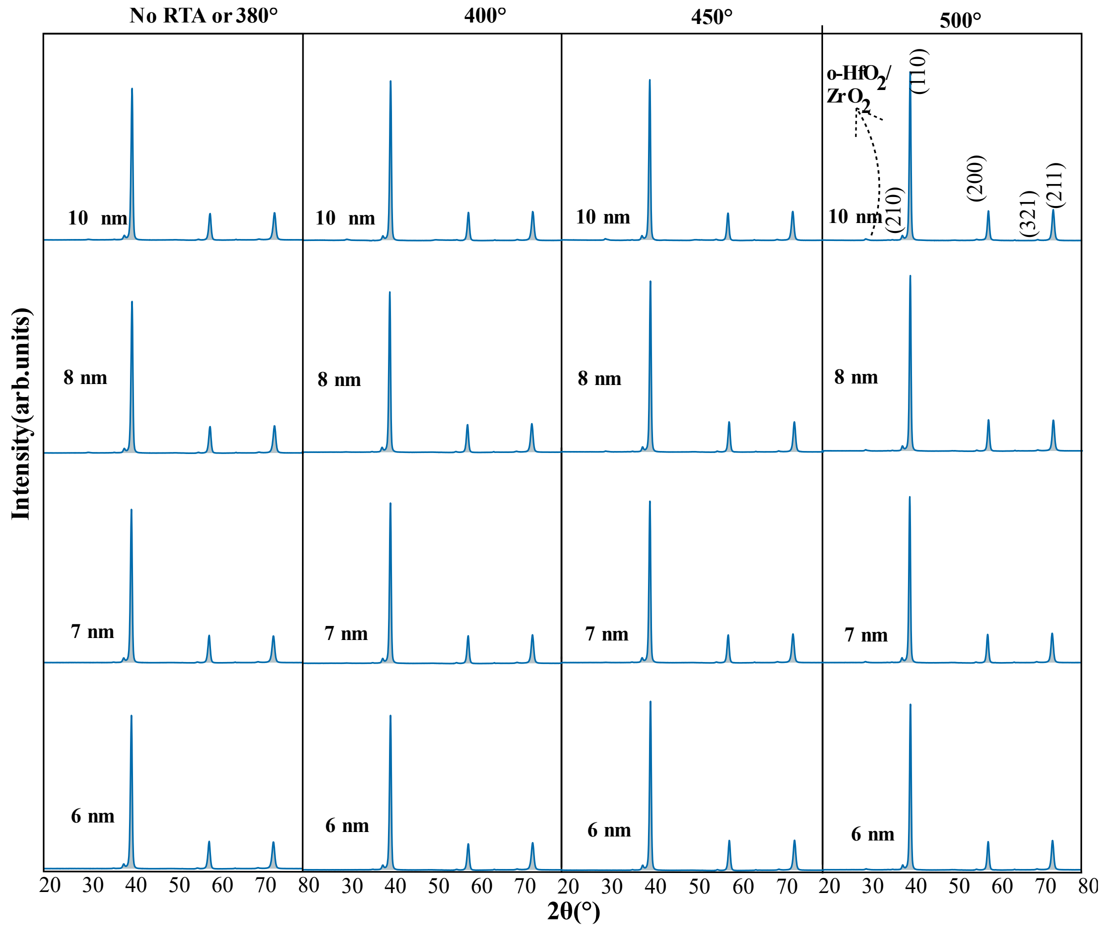

Figure 4.7: GIXRD spectra in 2θ range 20-80 (°) for the samples of $AR_{300/300}$.

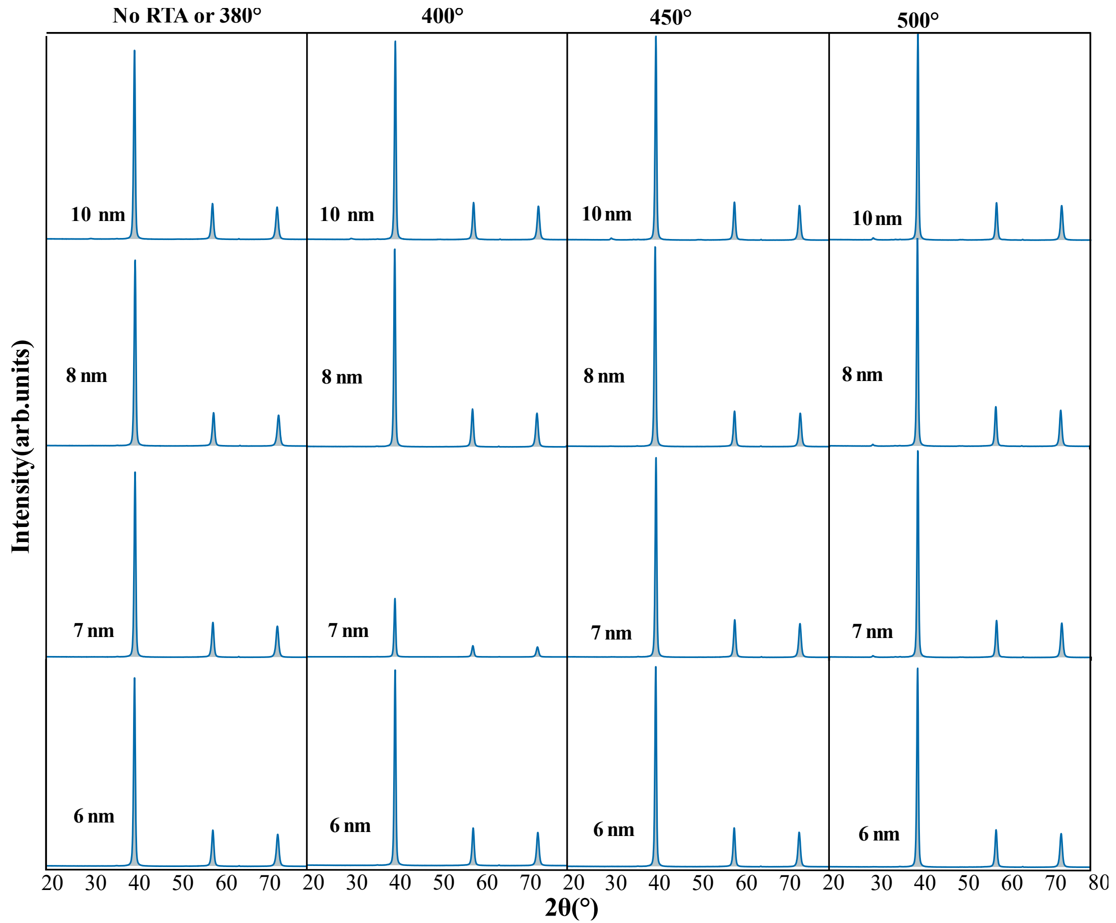

Figure 4.8: GIXRD spectra in 2θ range 20-80 (°) for the samples of $AR_{500/300}$.

These results are expected because the surface of all the samples is covered with a thick tungsten layer (~150 nm), which strongly scatters the X-ray beam. Since the HZO layer is much thinner (6-10 nm), its contribution to the diffraction pattern is small in this wide-angle range. However, a small peak around 2θ ≈ 30°, which corresponds to the orthorhombic ferroelectric phase of HZO, is still visible. Its lower intensity is not due to weak crystallization, but rather because it is partially hidden by the strong signal from the W layer.

To better identify the weak diffraction peak originating from the HZO layer, the GIXRD spectra in the 2θ range of 20°–80° were magnified by multiplying the intensity by a factor of 70. As shown in Figure 4.9, this zoomed view reveals the characteristic

orthorhombic HZO peak around 2θ ≈ 30°, which is otherwise barely visible in the original spectra presented in Figure 4.7 and Figure 4.8.

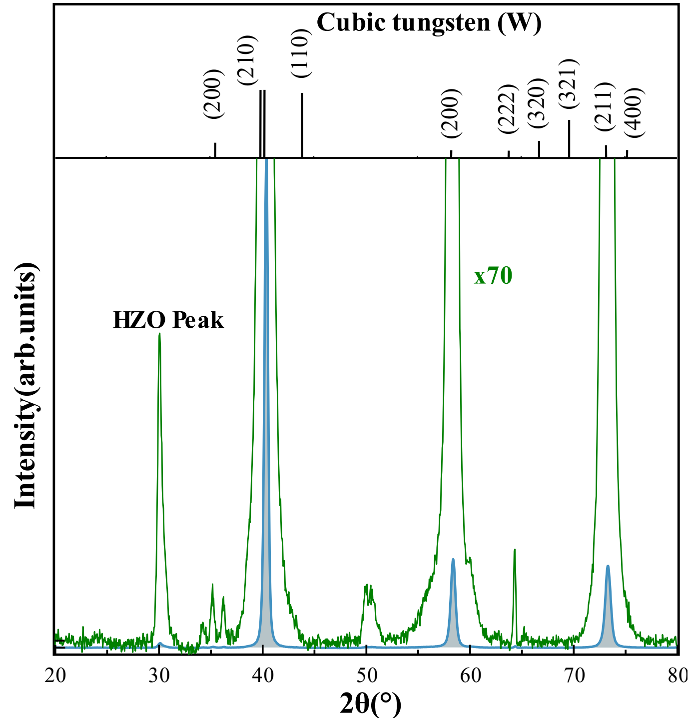

Figure 4.9: GIXRD spectra in (20-80)° range, with intensity curve of 70x of the original curve.

The diffraction patterns in Figure 4.7 and Figure 4.8 appear very similar across different HZO thicknesses and aspect ratios, confirming that the dominant peaks in this range originate from the W layer. Therefore, to better resolve and analyze the crystallization behavior of the HZO layer, a more detailed investigation was performed in narrower 2θ range of 27°–34°, where the characteristic HZO diffraction peaks are expected to appear.

Figure 4.10 describes the influence of the parameters: HZO Thickness, RTA temperature and aspect ratio on the evolution of GIXRD spectra measured with high resolution range (2θ is between 27° and 34°). Figure 4.10 (a-d) and Figure 4.10 (e-h) show measured GIXRD curves for the groups of samples with aspect ratios 500/300 and 300/300,

respectively. RTA temperatures of the measured samples were varied: no annealing or 380 °C, 400 °C, 450 °C, and 500 °C. HZO thickness for different measured samples also varied: 6nm, 7nm, 8nm, and 10nm.

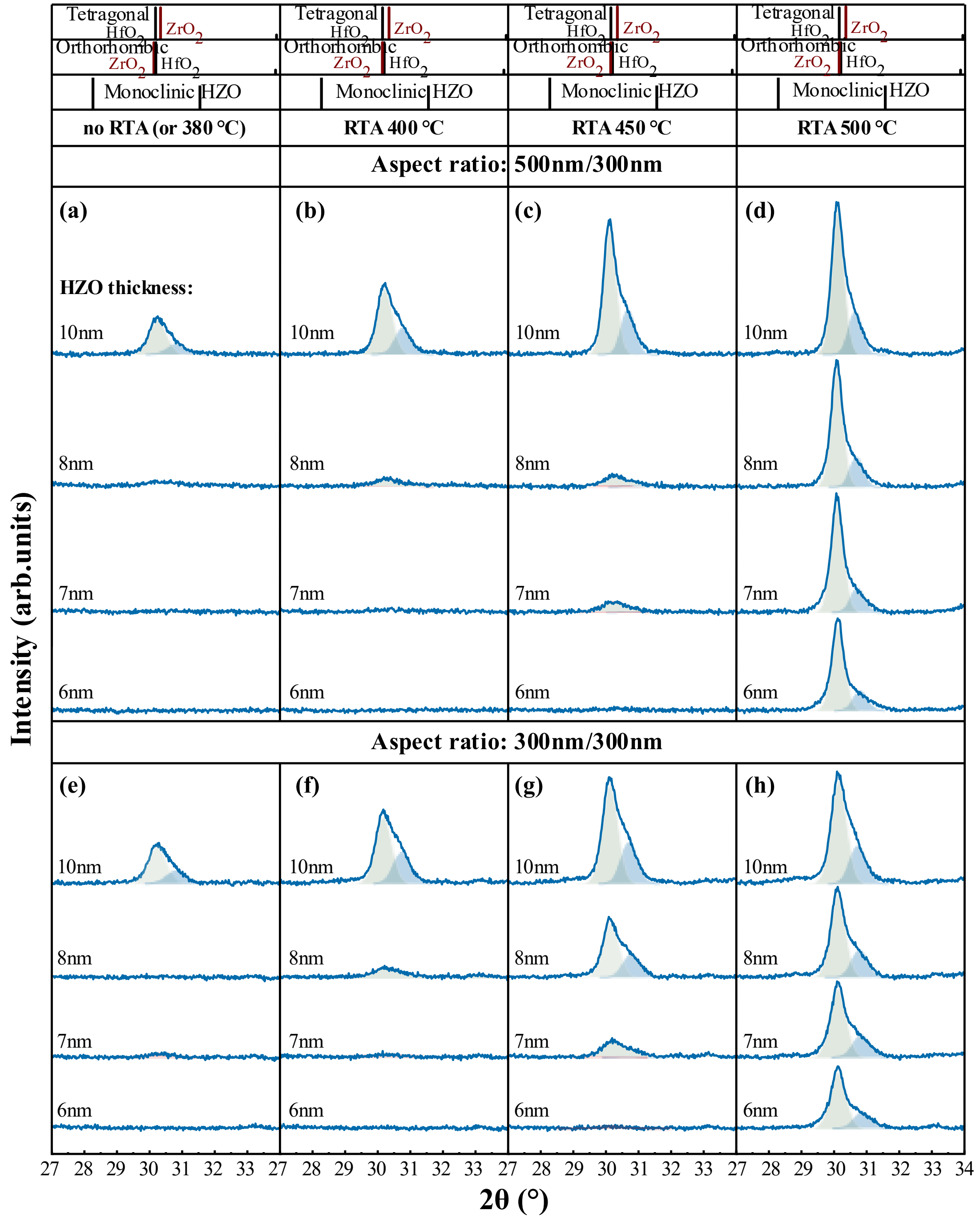

Figure 4.10: The GXRD patterns in the interested 2θ angle range 27°–34°.

The absence or weakness of the peaks in the left parts of the figure indicate that lower thickness of HZO need higher crystallization temperature to overcome the energy barriers associated with nucleation, interface effects, stress, and grain growth limitations (Hsain *et al*., 2020). On the other hand, It is observed that samples of higher aspect ratio exhibit higher peaks than samples of lower aspect ratio. This is attributed to the larger surface area of higher aspect ratio samples, which increases diffraction volume and lead to stronger diffraction peaks compared to lower aspect ratio samples.

The most controversial observation when compare between the two aspect ratio, that at RTA temperature equal 450 °C and 400 °C, the lower aspect ratio $AR_{300/300}$ samples are easier to be crystallized than the higher aspect ratio $AR_{500/300}$ samples for same HZO thickness and same RTA temperature. The difficulty in crystallizing higher aspect ratio $AR_{500/300}$ samples at the same RTA temperatures of 450 °C and 400 °C compared to lower aspect ratio $AR_{300/300}$ samples is likely due to several factors, which include higher internal stress in taller structures hinders crystallization, less efficient heat transfer and increased temperature gradients in high aspect ratio samples, increased surface energy stabilizing the amorphous phase, confinement effects that restrict grain growth and nucleation and differential stress relaxation, with higher aspect ratio structures less able to relax stress during annealing (Han *et al*., 2023).

These effects collectively make it more challenging for higher aspect ratio samples to achieve the energy state needed for crystallization. This behavior is observed at 400 °C and 450 °C but not at 500 °C. At 500 °C, the opposite behavior is observed because the higher thermal energy compensates for these limitations. The elevated temperature enables better stress relaxation, enhances grain boundary mobility, and overcomes energy barriers for nucleation and growth in high aspect ratio structures. leading to stronger diffraction peaks compared to $AR_{300/300}$ samples (Yun *et al*., 2024).

The GIXRD spectra were deconvoluted by decomposing the main peak into two overlapped peaks using Gaussian functions in order to determine the contribution of different crystalline phases. Figure 4.11 displays larger view of the deconvoluted peaks. In general, three crystalline phases are expected in HfO_2-based capacitor structure:

monoclinic, tetragonal and orthorhombic. There is no peak at position of standard monoclinic phase (located approximately at 28° and 32°).

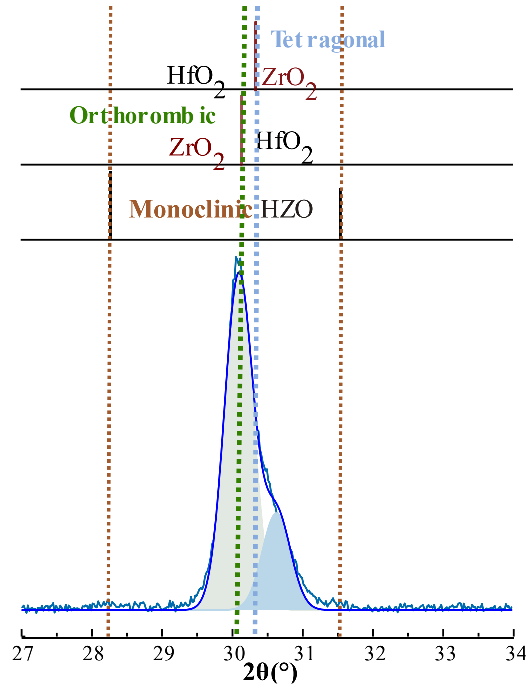

Figure 4.11 Crystalline phases in spectra of the studied structure.

The observed diffraction peaks grows around 2θ ~ 30.5, which is the position of HZO orthorhombic peak (Hashemi et al., 2021). In addition, Depending on the HfO_2 peak positions patterns at the top of the figure, (simulated from Huan et al. (2014)). the orthorhombic/tetragonal (o/t) HfO_2 phase lies around 2θ ~ 30.5. The left peak with a light green area which have higher intensity than the other right one, lies at 2θ equal 30.2° and represents the orthorhombic phase (or o-phase), likely associated with the non-centrosymmetric ferroelectric one. The right lower peak lies at 2θ equal 30.8° which associated with tetragonal non-ferroelectric phase (or t-phase) - a light blue area.

As Figure 4.10 (a-d) and Figure 4.10 (e-h) show, comparably high intensity tetragonal and orthorhombic XRD peaks are presented for the 10nm-thick HZO on the all RTA

temperature range and for the samples annealed at 500 ◦C in all HZO thickness range, this trends are similar for the groups of samples with aspect ratios 500/300 and 300/300.

For both groups of samples with different aspect ratios, o-, and t-phase XRD peak intensities increase as a function of thickness (for the fixed RTA temperature at 500 °C); also it increases as a function of RTA temperature (for a fixed HZO thickness at 10nm). Which mean enhancement of crystallization with increasing both of HZO thickness and RTA temperature.

For a better comparison of GIXRD results shown in Figure 4.10 (a-h), The integrated intensity of the left and right peaks was extracted from the figure and displayed in Figure 4.12 as a function of RTA Temperature and HZO thickness. Figure 4.12 (a) shows the integrated intensity as a function of RTA temperature measured for a 10-nm thick sample. Increasing RTA temperature, more HZO volume becomes crystalline, integrated peak intensity increases for the both peaks, and reaches a plateau in the temperature region [450-500]°C. Concerning thinner HZO samples (6nm, 7nm, and 8nm), it is possible to crystallize them at 500 °C, below this temperature there is a beginning at the crystallization temperature transition region.

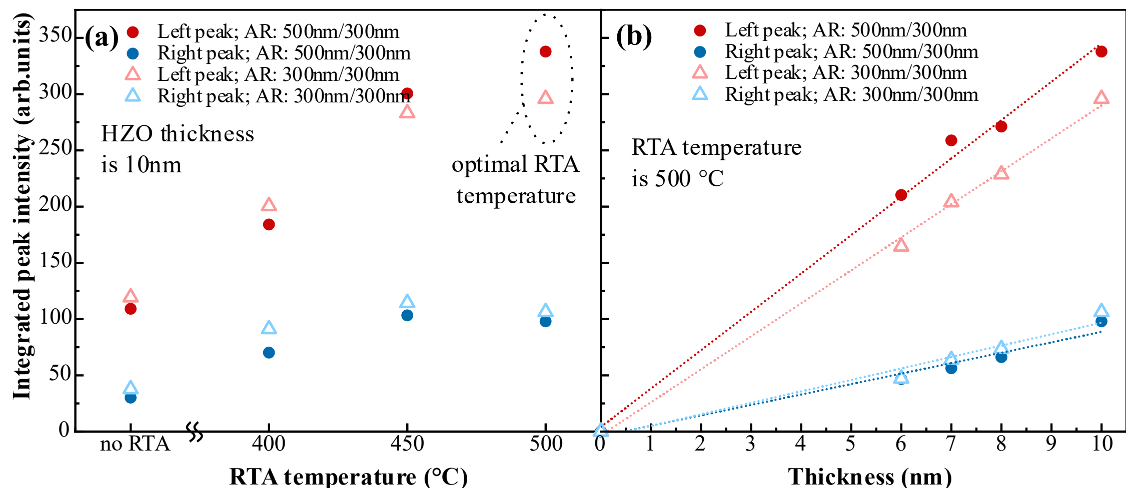

Figure 4.12: Integrated XRD peak intensity as a function of (a) RTA temperature. (b) HZO thickness; measured for the same type of samples, (a, b): integrated peak intensity for sample of $AR_{500/300}$ - closed circles, for sample of $AR_{300/300}$ -open triangles.

Thus, 500°C is the optimal temperature and to be able to compare two groups of samples with two different aspect ratios, RTA temperature 500°C had been chosen to study samples with different thicknesses and different aspect ratios. The ratio between the integrated o-XRD-peak intensities (left peak) values at 500 °C is 1.27 which roughly equal surface area ratio of the two 3D capacitor with different aspect ratio which was found in section 4.1.1.

Figure 4.12 (b) shows integrated peak intensities (in the 2θ-range [27-34]◦) for two sample aspect ratios (500/300 and 300/300) as a function of HZO layer thickness for the samples annealed at 500 °C for the left and right peaks. One can see, that o-XRD-peak (left peak) integrated intensity increases as a linear function of HZO thickness for both sample aspect ratios (500/300 and 300/300, Figure 4.12 (b).

For better visualization linear fit lines were added on the Figure 4.12 (b) (red and blue dashed lines with open and closed symbols). The slopes of these linear fit lines plotted for o-phase integrated peak intensities are different, the slope value is higher for the samples with an aspect ratio of 500/300. This is explained by the fact that the 3D measured area of the samples with an aspect ratio of 500/300 is higher than for the samples with an aspect ratio of 300/300. Then, since the XRD peak intensity is proportional to the amount of measured material, it is higher for the samples with higher surface area (with an aspect ratio of 500/300). For the right peak, the slopes of the linear fit lines are similar between the two aspect ratio samples, this behavior emphasis the non-ferroelectric nature of the right peak.

The ratio of integrated intensity area between the two aspect ratio samples when RTA temperature is 500 °C is determined at all HZO thicknesses and displayed in table 4.1. The value of the ratio which ranging from 1.2 to 1.36 indicate to consistency in enhancement of crystallinity when increase aspect ratio at different HZO thickness (6, 7, 8 and 10) nm, and it agrees with the surface area ratio of the two 3D capacitor with different aspect ratio which is calculated in section 4.1.1. These observations highlight the significance of both thickness and aspect ratio in determining the crystallization behavior of HZO thin films. The enhanced crystallinity in higher aspect ratio samples can be attributed to better surface

area effects, more effective stress relaxation, and favorable geometry for nucleation and grain growth.

Table 4.1: Integrated intensity area at RTA temperature equal 500 °C.

Thickness	Area($AR_{500/300}$)	Area($AR_{300/300}$)	Ratio
6	99.374	76.68185	1.29593
7	123.5479	90.6648	1.36269
8	127.7758	106.2351	1.20277
10	160.1858	126.1449	1.26986

4.3 Electrical Results Analysis

The electrical results of the studied devices are presented in this section. Capacitance-voltage, Current-voltage, PUND, and endurance measurements are used to describe ferroelectric behavior, switching dynamics, and long-term reliability. The influence of geometric and processing parameters on the devices' performance is discussed and described through analyzing the obtained electrical data.

4.3.1 Leakage Current Results

Current-Voltage measurements were performed for all the samples with different HZO thicknesses and different RTA temperature. Each sample was subjected to forward and reverse bias ramp reaches to ±5 V to measure breakdown voltage and current flow in the device. Figure 4.13 displays current density (J-V) characteristic of the samples with bias ramp between ±2. All the samples evidenced a leakage current density below 10^{-2} A/cm^2.

The initial increase in current observed at low bias does not correspond to steady leakage conduction but is influenced by transient displacement currents and trap-filling effects that occur immediately after bias application (Müller et al., 2012). Once these effects subside, the current stabilizes to a nearly constant value that reflects the true leakage. To

quantify leakage current from the J–V curves, the values are taken from the field region where the curves become flat before the onset of rapid current increase. As an example, for

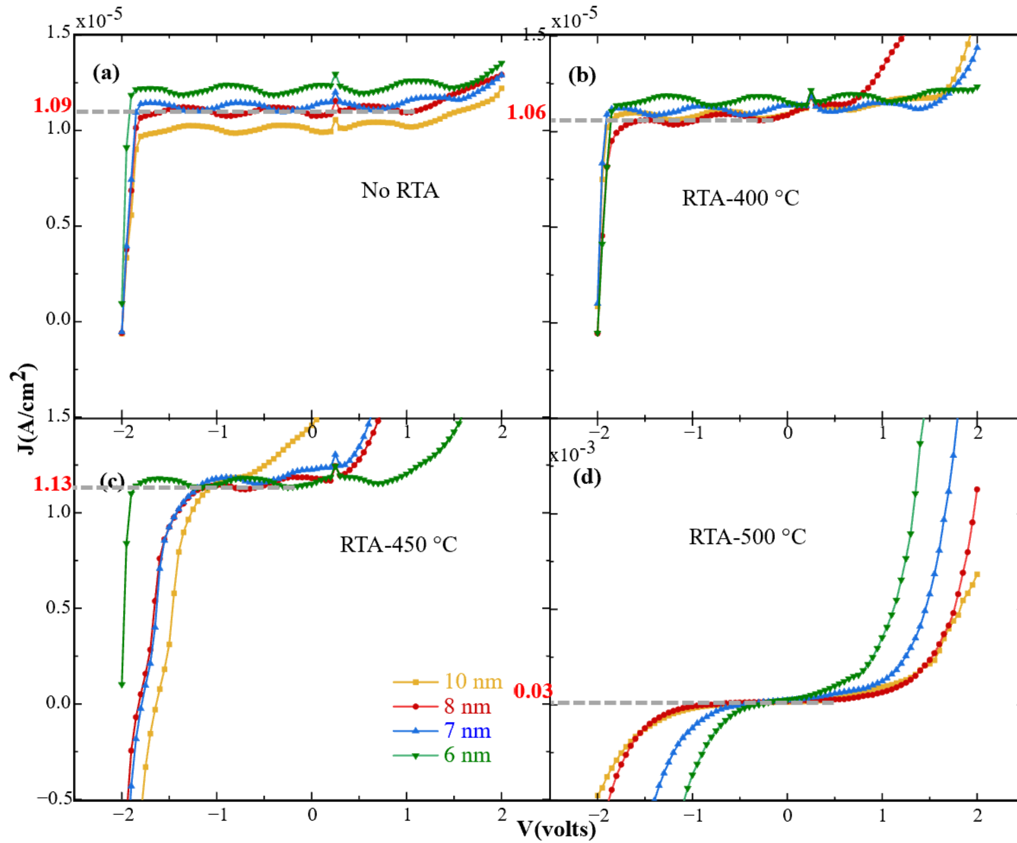

Figure 4.13: Current density as a function of voltage obtained on 3D HZO capacitors in case of (a) No RTA. (b) RTA-400 °C. (c) RTA-450 °C. (d) RTA-500 °C.

8 nm samples, the leakage current density is around 1.09X10^{-5} A/cm^2 (No RTA), 1.06X10^{-5} A/cm^2 (400°C), 1.13X10^{-5} A/cm^2 (450°C), 0.03X10^{-3} A/cm^2 (500°C), as shown in figure 4.13.

In addition, it is observable from the figure that the leakage increases with RTA temperature. The not annealed samples presenting smallest leakage compared to the annealed samples. In addition, it can be seen that voltage range for smallest leakage decrease with increasing RTA temperature; for example, the current start to increase significantly

around : 2 volts in case of RTA-400 °C (Figure 4.13 (b)), 1.5 volts in case of RTA-450 °C (Figure 4.13 (c)), and 1volts in case of RTA-500 °C (Figure 4.13 (d)).

The observed increase in leakage current density with higher RTA temperature can be attributed to thermally activated processes affecting the HZO layer and its interfaces. Annealing at elevated temperatures enhances crystallization of the HZO film, promoting the formation of the orthorhombic ferroelectric phase, which improves ferroelectric properties. However, it can also lead to an increase in defect density particularly oxygen vacancies due to enhanced diffusion and possible loss of oxygen from the film. Oxygen vacancies act as donor-like defects that create trap-assisted conduction pathways, facilitating leakage current under applied bias (Böscke *et al*., 2011).

The dependence of leakage current on HZO thickness shows different trends for 450 °C and 500 °C annealing temperature samples. At 450 °C (Figure 4.13 (c)), leakage increases with thickness, likely because thicker films contain more defects or incomplete crystallization, leading to additional leakage pathways (Park *et al*., 2013). In contrast, when RTA is 500 °C (Figure 4.13(d)), one can see that the leakage decreases with thickness.

Samples with 10 and 8 nm showed better current conduction compared to 7nm- and 6nm-thick (HZO) samples, which may be due to improved crystallinity and reduced defect density in thicker films annealed at this higher temperature. Thinner films at 500 °C may have higher concentrations of oxygen vacancies near interfaces, promoting trap-assisted conduction, while thicker films exhibit better grain growth and fewer leakage paths (Zagni *et al*., 2023).

4.3.2 Capacitance Voltage Characteristics

To better understand the dielectric response and ferroelectric behavior of the fabricated devices, C–V measurements were performed using the Aixacct system under different testing conditions. These measurements provide insight into the influence of frequency (Figure 4.14), applied voltage amplitude (Figure 4.15), and device aspect ratio (Figure 4.16) on the shape and magnitude of the butterfly curves. All measurements were

carried out on pristine 10 nm-thick HZO capacitors annealed at 500 °C, with the 2D surface area of the top W electrode set as the reference value, with a small-signal probing amplitude of 100 mV superimposed on the applied bias.

The obtained C–V curves exhibit the well-known butterfly shape, which is symmetric around a certain bias point close to 0 V. For consistency, the capacitance values reported in the following discussion are taken at this symmetry point (as indicated in the figures), since it represents the unbiased state of the device and allows direct comparison under different conditions.

Figure 4.14 shows the C–V characteristics of an $AR_{300/300}$ sample measured at two different frequencies, 10 kHz and 100 kHz, with fixed voltage amplitude of 3 V. At the symmetry point, the capacitance is about 0.33 nF at 10 kHz and increases to ~0.36 nF at 100 kHz. The frequency dependence can be attributed to different dynamic responses of ferroelectric domains under alternating fields.

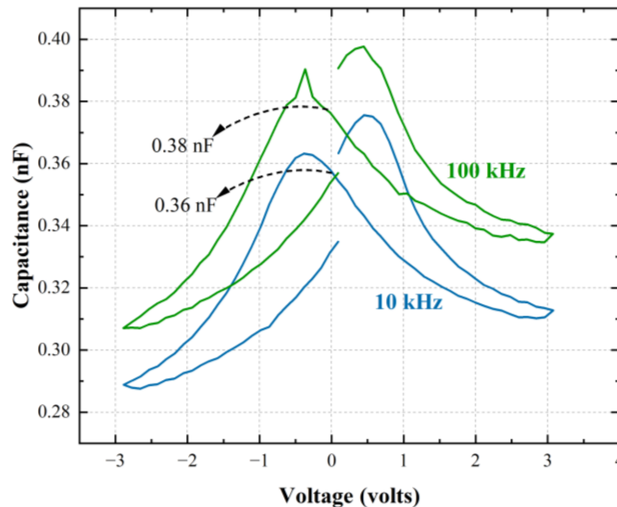

Figure 4.14: Capacitance-voltage curves at different frequencies, 10kHz (blue line) and 100kHz (green line) for sample of $AR_{300/300}$ at fixed voltage amplitude (3 V).

Figure 4.15 presents the C–V curves for the same sample measured with two different voltage amplitudes (2 V and 3 V) at a fixed frequency of 100 kHz. The higher driving voltage results in larger capacitance peaks, consistent with enhanced domain wall motion and polarization switching under stronger electric fields.

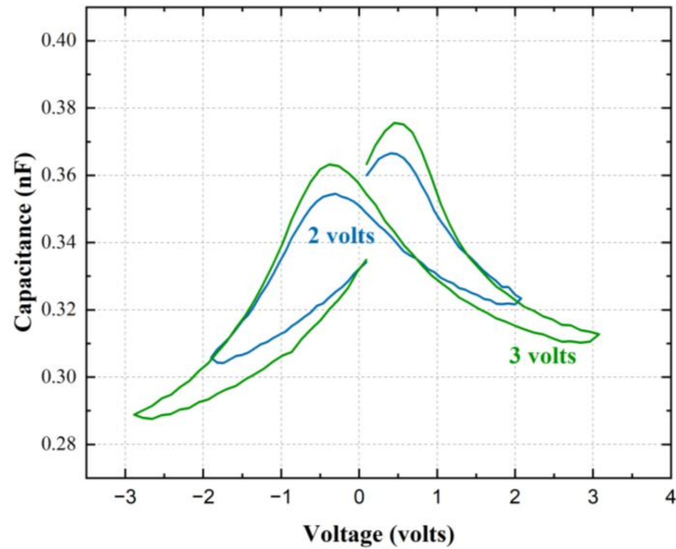

Figure 4.15: Capacitance-voltage curves at different voltage, 2V (blue line) and 3V (green line) for sample of $AR_{300/300}$ at 10 kHz.

Figure 4.16 compares two samples with different aspect ratios. The AR500/300 device (red curve) shows ~0.41 nF capacitance at the symmetry point, which is larger than the AR300/300 device (~0.34 nF). The ratio between the capacitances (~1.24) is close to the ratio of their top electrode areas calculated in Section 4.1.1, confirming that capacitance scales proportionally with electrode surface area.

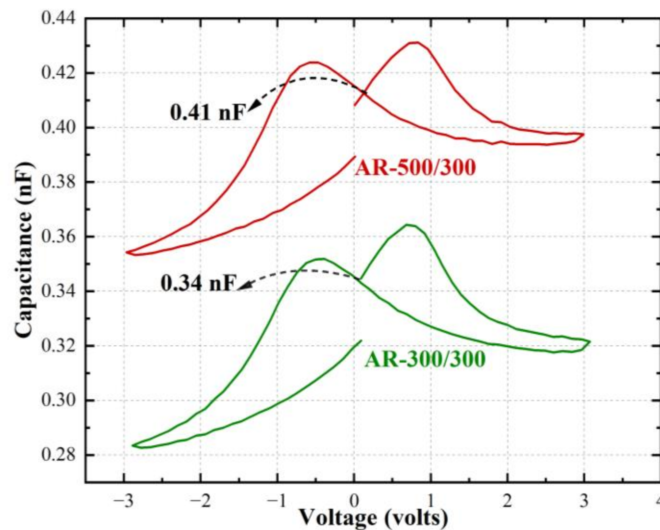

Figure 4.16: Capacitance-voltage curves for different AR samples, 500/300 (red line) and 300/300 (green line) at 10 kHz, 3V.

A theoretical reference capacitance was estimated with the parallel-plate model:

$$C = \varepsilon_0 \varepsilon_{\text{eff}} A/t \tag{4.4}$$

using the 2D surface area of the top W electrode (Aixacct "2D area" setting) and $t =$ 10nm. Matching the experimental capacitance at the symmetry point yields $\varepsilon_{\text{eff}} \approx 50$ for $AR_{300/300}$ ($C \approx 0.34$ nF) and ≈ 60 for $AR_{500/300}$ ($C \approx 0.41$ nF). These values are consistent with previously reported small-signal permittivity of ferroelectric HZO thin films (Schenk et al., 2014). and with the observed area scaling (the AR-500/300 to AR-300/300 capacitance ratio ≈ 1.24 matches the electrode-area ratio). The larger peak capacitance near the coercive voltages represents the maximum differential capacitance due to enhanced domain-wall response and is not used for baseline.

4.3.3 Dynamic Hysteresis Measurements Results

Dynamic hysteresis measurements were performed using a triangular waveform (p.61) with a voltage amplitude of 3V to evaluate the polarization switching behavior of the 10 nm HZO sample annealed at 500 °C with an aspect ratio of 500/300, with setting 2D surface area value of top W electrode on pristine devices. The loops were recorded at various frequencies: 1, 10, 50, and 100 kHz, as represented in Figure 4.17.

At 1 kHz, the hysteresis loop is well-formed and wide, indicating full polarization switching. As the frequency increases, the loops begin to narrow slightly, reflecting the dynamic response limitations of the material. Nevertheless, clear ferroelectric behavior is retained even at 100 kHz, confirming the device's ability to sustain polarization switching at high frequencies which is important for endurance testing.

The measured loops show consistent polarization values across the three cycles (P1, P2, and P3), suggesting stable switching behavior under repeated application of the triangular wave form. In addition, the symmetry of the loops indicate that the devices have

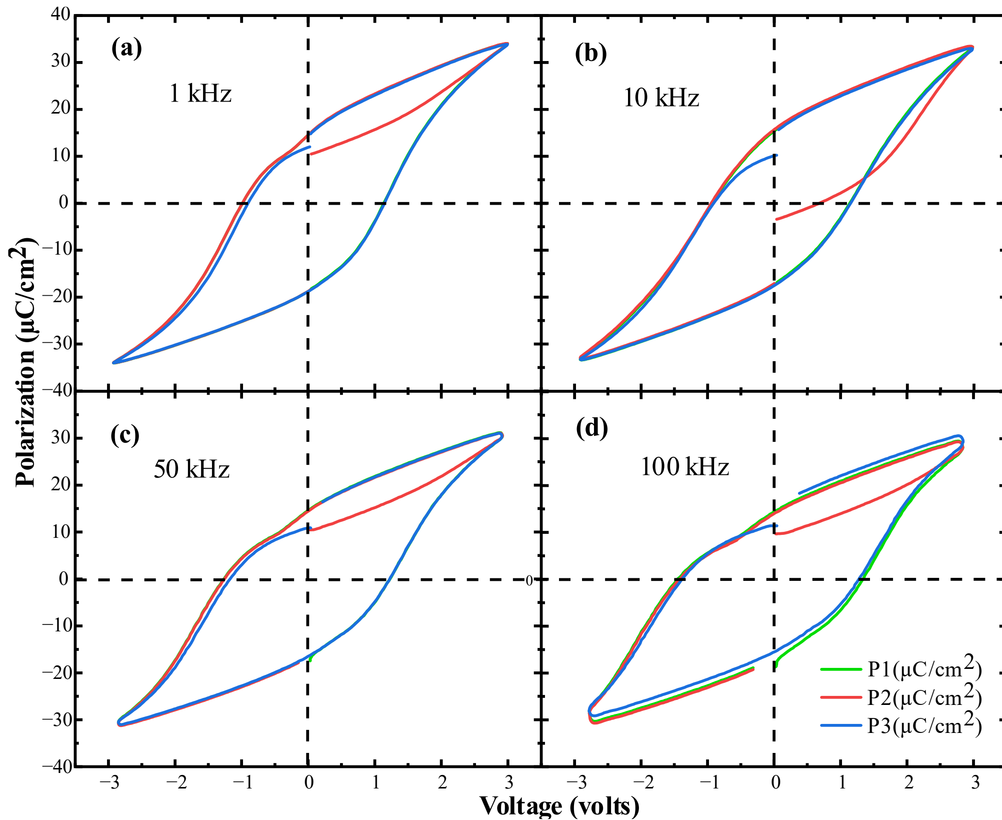

Figure 4.17: DHM loops for sample of 10 nm, 500 °C, $AR_{500/300}$ at different frequencies (a) 1 kHz. (b) 10 kHz. (c) 50 kHz. (d) 100 kHz; Voltage amplitude is set at 3 volts.

balanced switching behavior with minimal imprint or built-in electric field bias (Dawber *et al*., 2005).

4.3.4 PUND Results

This subsection presents the results obtained from PUND measurements (p.60) performed to evaluate the ferroelectric switching behavior of the TiN/HZO/TiN capacitors. The PUND technique enables accurate extraction of the intrinsic ferroelectric response by separating the switchable polarization from non-switchable contributions such as capacitive and leakage effects.

Throughout this study, PUND experiments were carried out using a standardized set of measurement parameters to ensure comparability between different samples. Unless

otherwise specified (*e.g.,* in frequency- or field-dependence studies), the following settings were applied: pulse frequency was fixed at 10 kHz, pulse shape was triangular, write and read pulse delays were both set to 1 s, and the write pulse time and rise time were each set to 25 µs. These values were proven based on some preliminary optimization measurements. For example, an experiment on delay read time was performed and showed that 1s is best value to obtain stable, saturated hysteresis loops.

The PUND amplitude was adjusted according to the HZO thickness to maintain a constant electric field of 4 or 3 MV/cm across all samples. The current range was also selected based on the expected switching current, typically set to 1 mA for standard measurements.

4.3.3.1 Effect of Electric Field on the Ferroelectric Behavior

To evaluate the optimal operating conditions for the devices and to support parameter selection for subsequent measurements, the influence of electric field amplitude on the ferroelectric response of HZO capacitors was systematically examined. This preliminary experiment was performed to determine the minimum electric field required to induce clear polarization switching without reaching dielectric breakdown. For each HZO thickness, the applied voltage was adjusted to achieve a range of electric fields from 2 MV/cm to 7 MV/cm. Table 4.2 provides the corresponding voltage values for each thickness.

Table 4.2: Electric field calibration for HZO capacitors with Varying HZO thicknesses.

Thickness	**10nm**	**8 nm**	**7 nm**	**6 nm**
Electric field (MV/cm)	**Applied voltage (V)**			
2	2.0	1.6	1.4	1.2
3	3.0	2.4	2.1	1.8
4	4.0	3.2	2.8	2.4
5	5.0	4.0	3.5	3.0
6	6.0	4.8	4.2	3.6
7	7.0	5.6	4.9	4.2

Figure 4.18 and Figure 4.19 display the hysteresis loops obtained from samples with aspect ratios $AR_{500/300}$ and $AR_{300/300}$, respectively, measured using PUND method at a frequency of 10 kHz. These figures show the evolution of the polarization loops as a function of electric field under different RTA temperatures for HZO layers of 6 to10 nm. The loops become more well-defined and square-shaped with increasing electric field, indicating enhanced polarization switching. This effect is particularly visible in the 10 nm samples, where saturation is more clearly reached at fields above 4 MV/cm.

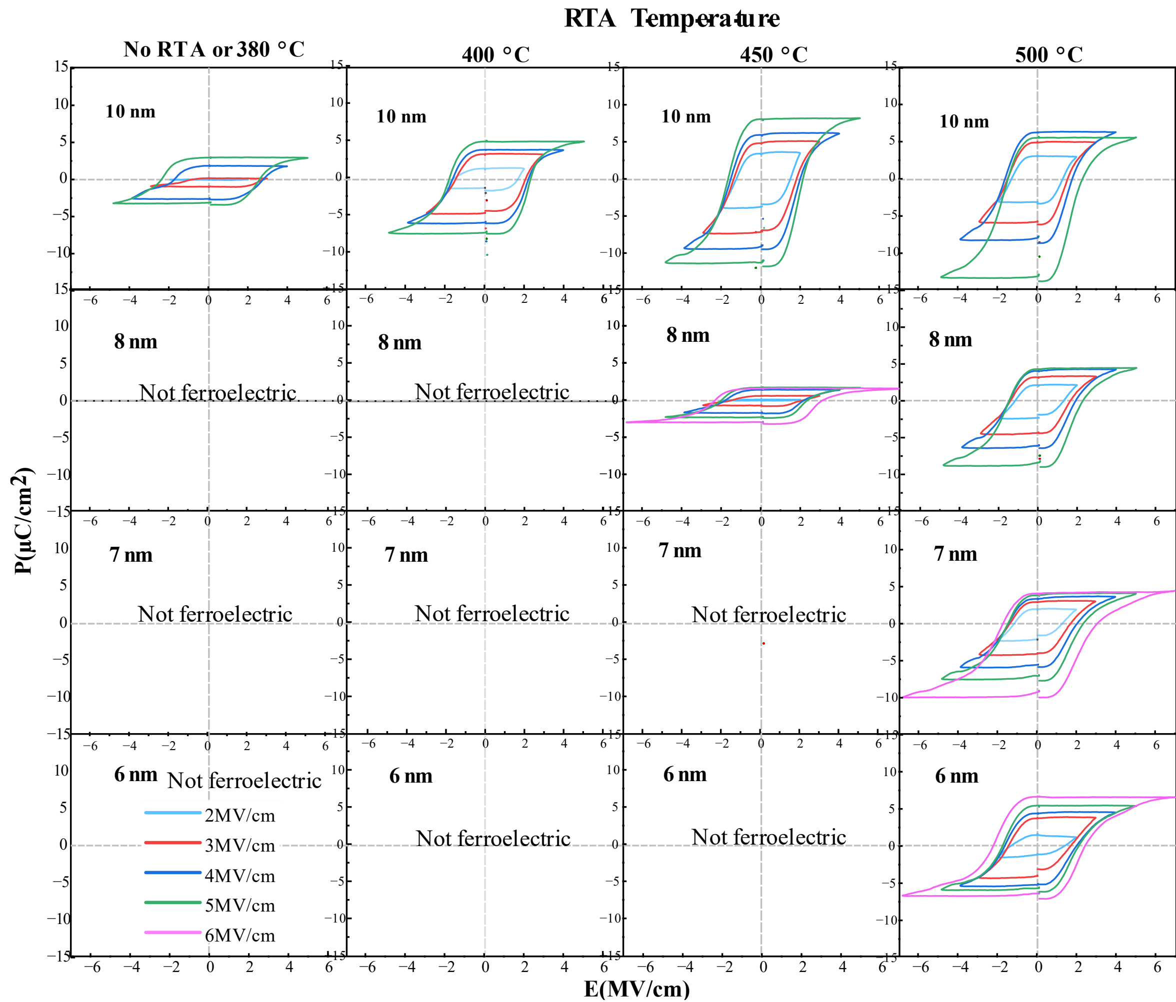

Figure 4.18: Hysteresis loops at different electric fields for samples of $AR_{500/300}$; PUND frequency equal 10 kHz.

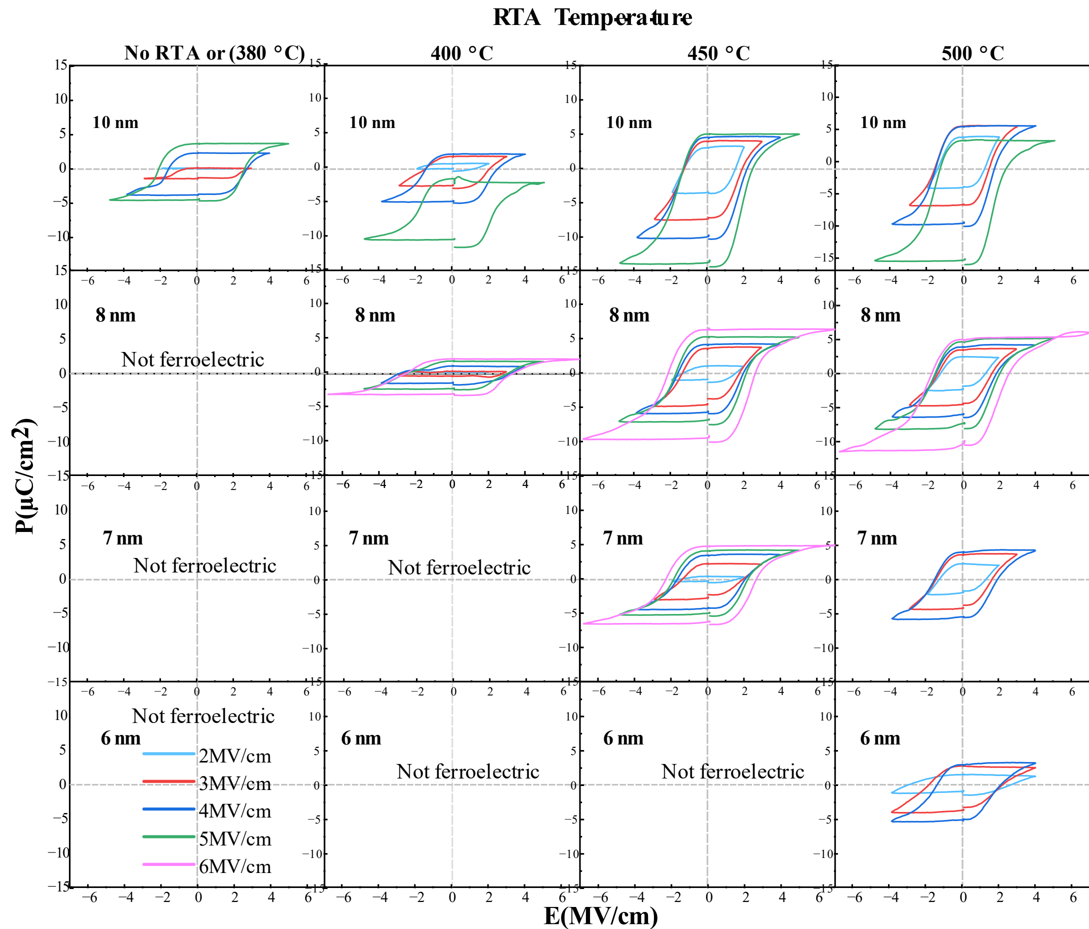

Figure 4.19: Hysteresis loops at different electric fields for samples of $AR_{300/300}$; PUND frequency equal 10 kHz.

The coercive field can be estimated from the loops and was found to vary between 1.8–2.5 MV/cm depending on thickness and annealing temperature. As observed in literature, the coercive field tends to increase slightly with reduced thickness (Alrifai, 2024). these consistent with the stronger depolarizing field and greater domain pinning expected in ultrathin ferroelectric layers.

Figure 4.19 provides a parallel view of the same experiment, but now for $AR_{300/300}$ samples. In general, the polarization loops follow the same trends observed in Figure 4.18, although with slightly lower maximum polarization values. For both aspect ratios, ferroelectric switching is absent in not-annealed samples with HZO thickness ≤ 8 nm, indicating that thermal treatment is necessary to stabilize the ferroelectric phase in thinner

films. At RTA temperature 500 °C, clear hysteresis loops appear even for the 6 nm films, particularly under higher electric fields (≥ 5 MV/cm), which confirms the influence of annealing and thermal energy in promoting the orthorhombic phase formation.

Additionally, it is observable that breakdown voltage decrease with increasing HZO thickness: thinner films like 6 and 7 nm could sustain fields up to 6–7 MV/cm, while 10 nm samples typically broke down around 6 MV/cm. This inverse relationship between thickness and breakdown field is consistent with findings in previous studies (Böscke et al., 2011; Müller et al., 2012; Zagni et al., 2023).

In conclusion, this electric field dependence study demonstrates that an applied field of approximately 3–4 MV/cm is sufficient to induce robust ferroelectric switching in all annealed samples with HZO thicknesses from 6 to 10 nm. It also confirms that both annealing temperature and geometric design (aspect ratio) influence the switching strength and breakdown tolerance. Electric field values of 3 MV/cm, and 4 MV/cm were selected as optimal values to apply it on the PUND experiments for studying effect of the main three parameters: Aspect ratio, HZO thickness and RTA temperature on the ferroelectric behavior of the devices.

4.3.3.2 Effect of PUND Frequency on the Ferroelectric Behavior

To evaluate the effect of switching speed on the polarization behavior, a frequency-dependent PUND experiment was conducted on all the fabricated samples. The aim was to identify an optimal frequency for accurate and stable measurement. Although the test was performed for all samples, only the results for the devices that exhibited the most stable and representative loops are shown in Figure 4.20. The selected samples contains a 10 nm HZO layer annealed at 450 °C, with two different aspect ratios ($AR_{500/300}$ and $AR_{300/300}$) displayed side by side.

The PUND measurements were performed at five frequencies: 1 kHz, 5 kHz, 10 kHz, 25 kHz, and 50 kHz. These frequencies were set by adjusting the rise time of the triangular waveform used in the pulse sequence. The influence of frequency is reflected in the loop

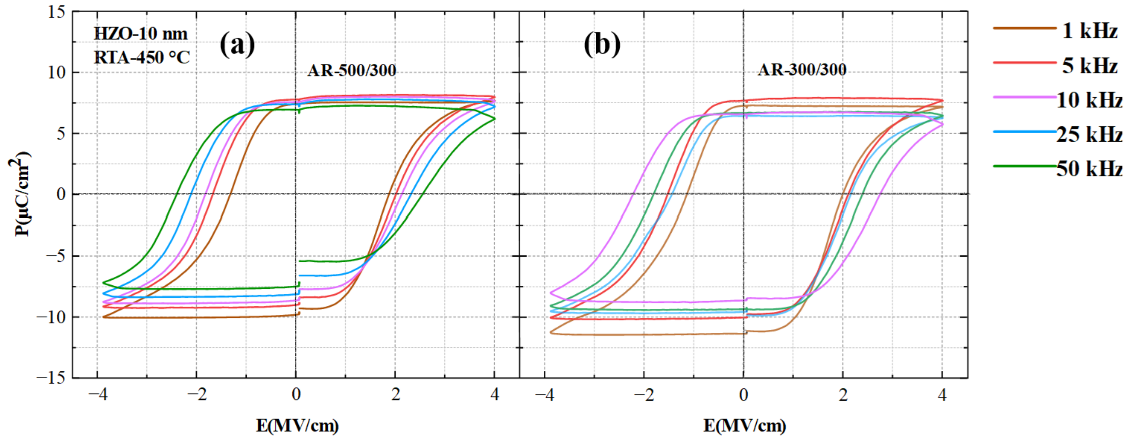

Figure 4.20: Hysteresis loops at different PUND frequencies for samples of 10 nm HZO, RTA-450 °C: (a) $AR_{500/300}$ (b)$AR_{300/300}$.

shape and the coercive electric field. As frequency increases, loops exhibit slightly narrower profiles and a small increase in E_C, which can be attributed to incomplete switching at shorter pulse durations. The remanent polarization remains nearly unchanged, demonstrating stable switching behavior up to 50 kHz.

An important observation during these measurements was the change in current range required by the test system as a function of frequency. At low frequency (1 kHz), the current range required was 100 µA, while higher frequencies (5–25 kHz) required 1 mA, and the highest frequency tested (50 kHz) required 10 mA. This reflects the increased current needed to support faster charge displacement during rapid polarization switching. The details of the applied PUND parameters are summarized in Table 4.3.

Table 4.3: PUND frequency settings with corresponding rise time and current range used in polarization measurements.

PUND frequency (kHz)	Rise time (µs)	Current range (mA)
1	250	0.1
5	50	1
10	25	1
25	10	10

Additionally, it is important to clarify that performing PUND measurements at high enough frequency with fast switching speed is important to minimize the effect of leakage current and ensures that the measured polarization primarily reflects the true switching current. In this work, a frequency of 10 kHz was selected as an optimal cooperation: it is high enough to suppress leakage contributions, while still allowing reliable switching of the ferroelectric domains and stable operation of the measurement system. This choice is consistent with previous studies that have reported accurate extraction of remanent polarization at similar frequencies (Skopin *et al*., 2022).

4.3.3.3 Hysteresis Loops at 10 kHz, 3MV/cm

After investigating the role of PUND frequency and the applied electric field on the switching behavior of the devices, PUND measurements with electric field equal 3MV/cm and frequency equal 10 kHz were performed on all the samples. Figure 4.21 shows P-E characteristics, measured for the samples with different HZO thicknesses (6nm, 7nm, 8nm, and 10nm) and annealed at various temperatures (400 °C, 450 °C, 500 °C; and not annealed samples). Another varied parameter was the sample aspect ratio: 500/300 (red lines) and 300/300 (green lines).

As expected, based on GIXRD results (Figure 4.10), hysteresis loops are presented for the 10 nm-thick HZO samples annealed at different temperatures and for the samples with thicknesses 6nm, 7nm, 8nm, and 10nm; annealed at 500 °C; for the samples with both aspect rations. It is observed that the loops expand in window when RTA temperature increases, for both aspect ratio samples. In addition, the loops expand with increasing HZO thickness, but the effect of HZO thickness is limited compared to the effect of increasing the annealing temperature.

To understand physical interpretation of these observations, it is reported that enhancement of ferroelectric behavior with increasing RTA temperature is achieved by reducing defects, and stabilizing the orthorhombic phase (Gronenberg *et al.,* 2022).

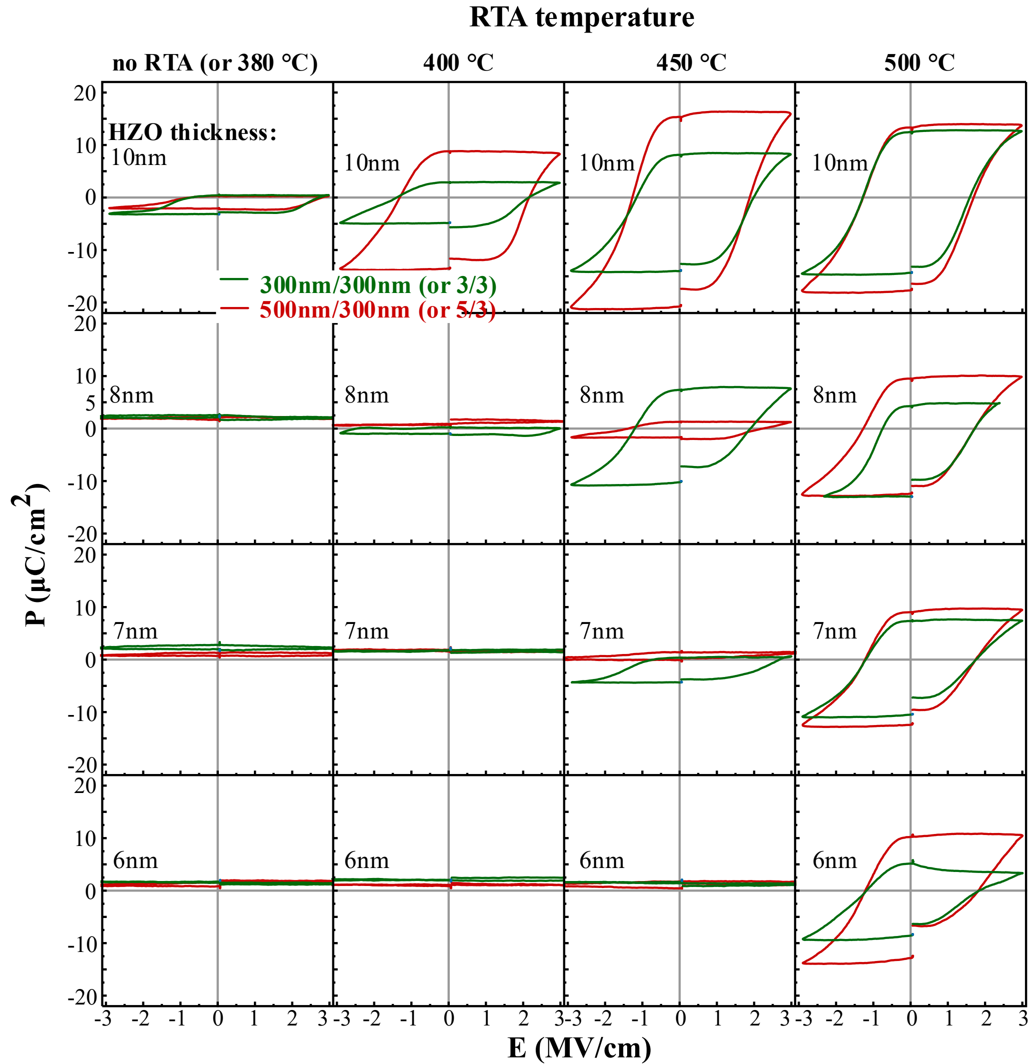

Figure 4.21: Polarization as a function of the electric field (P–E) characteristics obtained for pristine devices of 3D TiN/HZO/TiN structures with different HZO thicknesses and different RTA temperature for the two aspect ratio samples.

Additionally, thicker HZO layers improve polarization due to increased ferroelectric material volume (Saha *et al.,* 2021).

Since, the area value of the contact, used for plotting polarization P on Figure 4.21, was W circle area (2D), not an HZO area (3D), it is expected a higher polarization window for the samples of $AR_{500/300}$ than for the samples of $AR_{300/300}$. Almost for all measured samples $2P_r$ value for the samples with aspect ratio 500/300 is higher than for the samples with an aspect ratio 300/300. Exceptionally, for lower HZO thickness and lower RTA

temperature, the polarization window is higher for the samples with lower aspect ratio: 8nm, 7nm-thick samples annealed at 450 °C. This can be explained by the fact that annealing temperature of this sample is at the beginning of the crystallization transition annealing temperature range, and the thickness error becomes an important parameter.

For the rest of the samples, the polarization window is not observed: samples of 8 nm not-annealed and annealed at 400 °C, samples of 7nm HZO not-annealed and annealed at 400 °C, samples of 6nm HZO not-annealed and annealed at 400 °C, 450 °C. These samples with $2P_r \sim 0$, were annealed at the RTA temperatures, which are below the temperature at which the crystallization transition temperature range starts. These results are in correlation with GIXRD measurements.

Another important parameter is the coercive field E_c, the E_c value is almost the same for two samples with different aspect ratios but with the sample with same HZO thickness and same RTA temperature. For the studied samples with visible hysteresis loop, the positive E_c is in the range [1.6-2.2]V, and the negative E_c is in the range [(-1.4)-(-1.2)]V. This difference can be explained by a small shift of hysteresis loops of the P-axis to the negative direction.

The values of $2P_r$ were extracted from the loops in Figure 4.21 and represented as a function of RTA temperature and HZO thickness in Figure 4.22. It is observed from the figure that $2P_r$ values increases with both RTA temperature and HZO thickness. In (Figure 4.22 (a)), the values of $2P_r$ increase with RTA temperature and starts to reach a plateau in the temperature region [450 - 500] °C. In addition, the figure proves that samples with higher AR exhibit higher values of $2P_r$ than the lower AR samples at different RTA temperature. However, not annealed samples of both aspect ratio show similar value of $2P_r$. This behavior suggests that before RTA treatment, both samples remain largely amorphous, with minimal crystallization and ferroelectricity.

In (Figure 4.22 (b)), Liner fit lines was added for the samples with different aspect ratios (red and green dashed lines). The slope of the line plotted for the samples with an

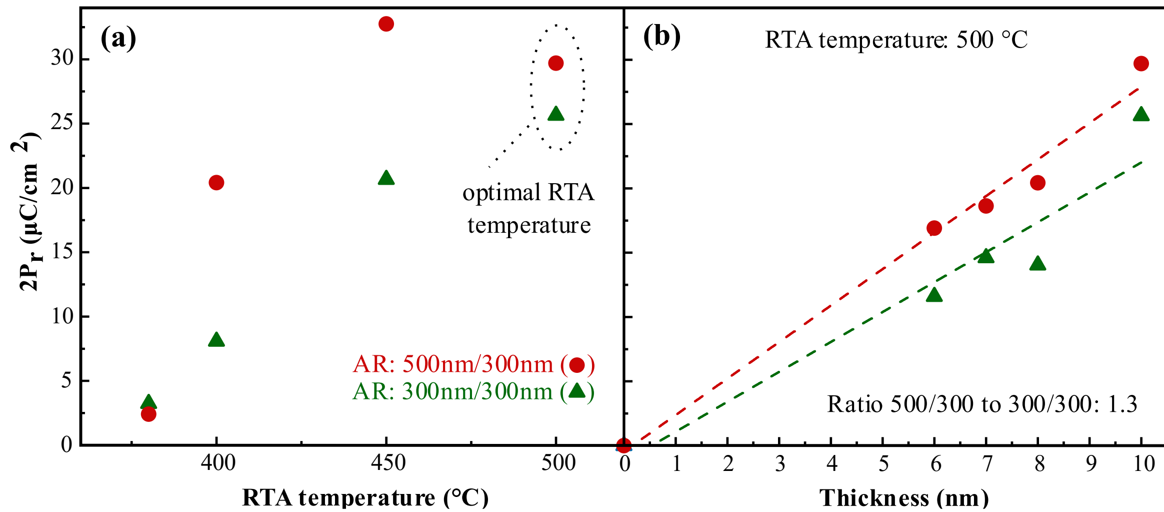

Figure 4.22: $2P_r$ values as a function of (a) RTA temperature (b) HZO thickness.

aspect ratio of 500/300 is higher than for the line plotted for the samples with an aspect ratio of 300/300. This difference is due to the way of calculating the P value, it was normalized by 2D W contact surface area, but not by 3D HZO surface area. The measured ratio between two $2P_r$ *vs* HZO thickness slopes (for two surface sample types aspect ratios) is 1.3, which is the same as the ratio of $S_{3D500/300}$ to $S_{3D300/300}$ which is calculated in section 4.1.1.

This result confirms, that for the 6nm, 7nm, 8nm, and 10nm thick HZO samples analyzed at 500 °C, it is possible to see a clear difference between the samples with two different aspect ratios. Increasing 3D aspect ratio of the 3D substrate, obtained ferroelectric HZO with a higher polarization value. This polarization value was proportional to the surface area.

4.3.5 Endurance Results

The effect of the three parameters HZO thickness, RTA temperature, and aspect ratio on the endurance performance of 3D HZO capacitors under cycling at two different frequencies: 1 kHz (open symbols) and 100 kHz (closed symbols) are displayed in Figure 4.23.

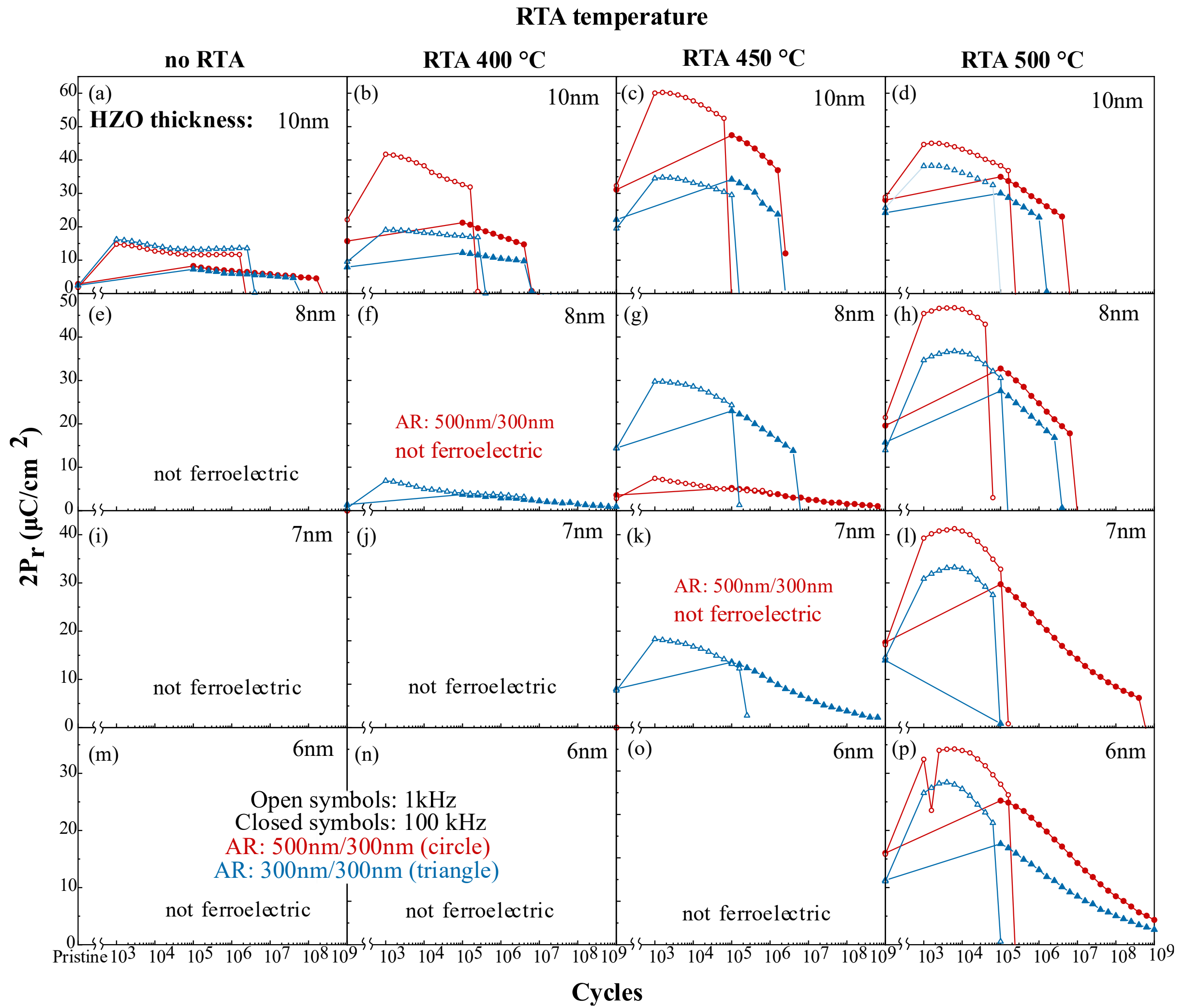

Figure 4.23: Endurance measurement at two cycling frequencies frequency; 1KHz and 100KHz, for all the samples at different HZO thickness and different RTA temperature; closed symbols (100 kHz), open symbols (1kHz).

At the beginning of the cycling, an immediate strong polarization wake-up is observed, characterized by an increase in remanent polarization as defects and domains align under electrical cycling. However, as cycling continues, all devices eventually undergo fatigue, with a gradual decline in $2P_r$ values until electrical breakdown occurs.

As electrical cycling progresses, the repeated switching of ferroelectric domains leads to structural and interfacial changes within the HZO layer. Over time, defects such as oxygen vacancies and charge traps accumulate, particularly at interfaces, and begin to

pin domain walls or partially block polarization switching. This gradual degradation in switching capability is referred to as ferroelectric fatigue (Yingwei *et al.,* 2020). As a result, the remanent polarization decreases with continued cycling. In advanced stages, localized leakage pathways may form due to defect clustering or dielectric damage, eventually causing electrical breakdown (Böscke *et al.,* 2011).

Samples with lower HZO thickness and lower RTA temperatures consistently demonstrate better endurance performance compared to thicker and higher-temperature samples. For example, the endurance extends up to 10^9 cycles for thinner samples such as 6 nm at 500 °C, 7 nm at 450 °C, 8 nm at 400 °C; highlighting that reduced thickness and moderate annealing temperatures mitigate fatigue effects. These results agree with the fact that thinner films exhibit fewer defects and reduced stress gradients, which lead to better charge retention and domain stability over extended cycling (Xiao *et al*., 2011).

Similarly, moderate RTA temperatures improve the crystallinity and defect density of the HZO layer without introducing excessive stresses or leakage paths, which could degrade endurance. For the same RTA temperature and HZO thickness, samples with higher aspect ratios ($AR_{500/300}$) exhibit higher value of endurance compared to lower aspect ratio ($AR_{300/300}$) samples. This behavior is likely attributed to the larger surface area and better electric field distribution in higher aspect ratio structures, which enhance domain switching and reduce localized fatigue.

Furthermore, the cycling frequency significantly influences both polarization and endurance: the $2P_r$ values are larger at 1 kHz due to the slower switching dynamics allowing more complete domain alignment, whereas cycling at 100 kHz demonstrates improved endurance because the faster cycling induces less charge trapping and reduces the time available for fatigue-related degradation mechanisms. Charge trapping refers to the accumulation of injected charges such as electrons or holes at interfaces or within defects in the HZO layer (Debucquoy et al., 2009).

Figure 4.24 displays the endurance result at 100 kHz for the sample which demonstrated the biggest opening of the hysteresis loop. At the beginning of the cycling,

an immediate strong polarization wake-up is observed, characterized by an increase in remanent polarization (10^5 cycles). However, as cycling continues (10^5-10^6cycles), $2P_r$ starts to decrease (fatigue), and finally drops down at 10^6 cycles. The same behavior is observed for both sample aspect ratios: 500/300 and 300/300. The ratio between $2P_r$ measured for two samples [$2P_r$(500/300)] / [$2P_r$(300/300)] stays the same 1.4-1.5 for different numbers of cycles.

In the previous reports of Grenouillet *et al.,* it was shown that 3D-integrated HZO capacitors (10nm-thick HZO) demonstrate 1.3 times higher $2P_r$ values compared to 2D HZO capacitors. It should be noticed that different annealing procedures and different types of measurements are used by Grenouillet *et al*. Despite this difference, the present results are complementary to this study, and the study show that by increasing the 3D effective surface, it is possible to increase proportionally $2P_r$ values and keep the same endurance properties.

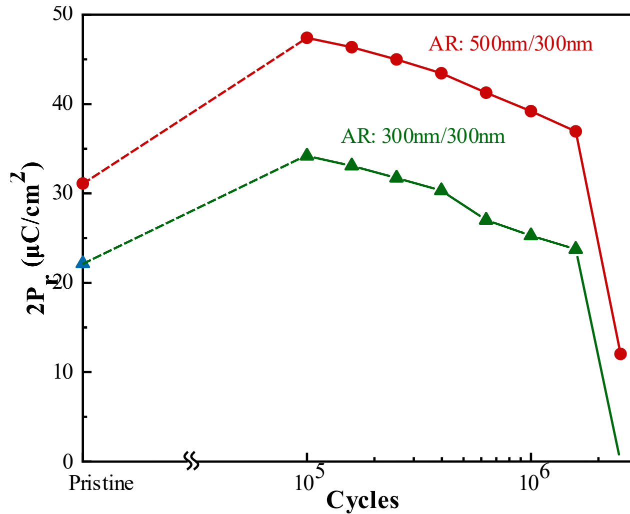

Figure 4.24: Endurance measurements at 100 kHz: $2P_r$ vs cycles, measured for the 10nm-thick HZO samples, annealed at 450 ◦C; measurements were performed for the samples with two aspect ratios: 500/300 (red filled circles) and 300/300 (green filled triangles).

The evolution of P–E hysteresis loops for samples with an aspect ratio of 300/300 and 500/300 during electrical cycling at a frequency of 1 kHz is displayed in Figure 4.25 and Figure 4.26, respectively.

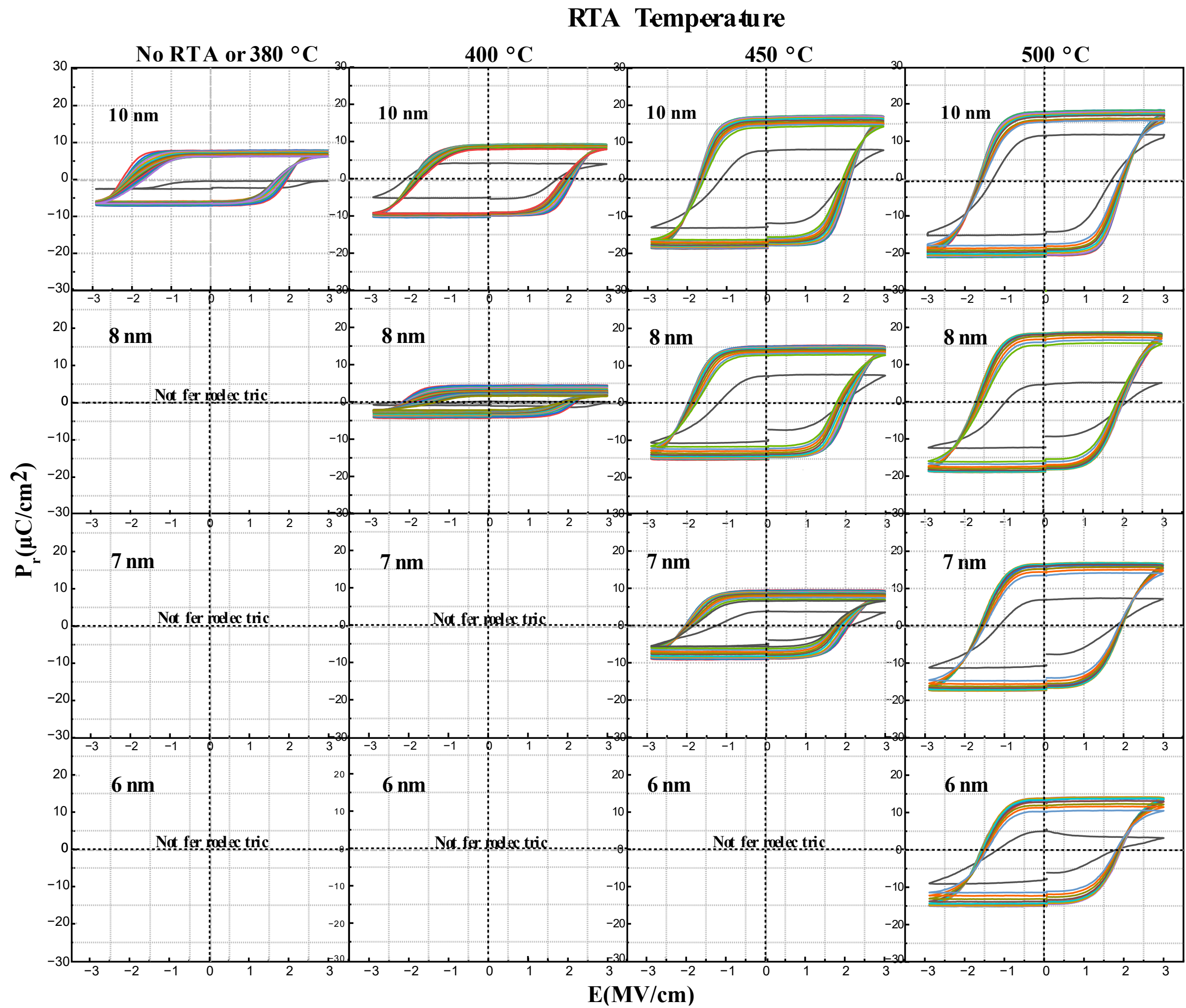

Figure 4.25: evolution of P–V hysteresis loops for samples with an aspect ratio of 300/300 during electrical cycling up to 10^9 cycles; at a frequency of 1 kHz.

The observations demonstrate the ferroelectric switching behavior throughout cycling and are presented for several HZO thicknesses ranging from 6 nm to 10 nm. Several samples (most notably the 10 nm and 8 nm HZO thicknesses) show distinct hysteresis loops with distinctive ferroelectric geometries in the initial pristine condition. The form of the loop gradually changes as the number of cycles rises; tiredness is indicated by an initial increase in polarization followed by a narrowing of the loop.

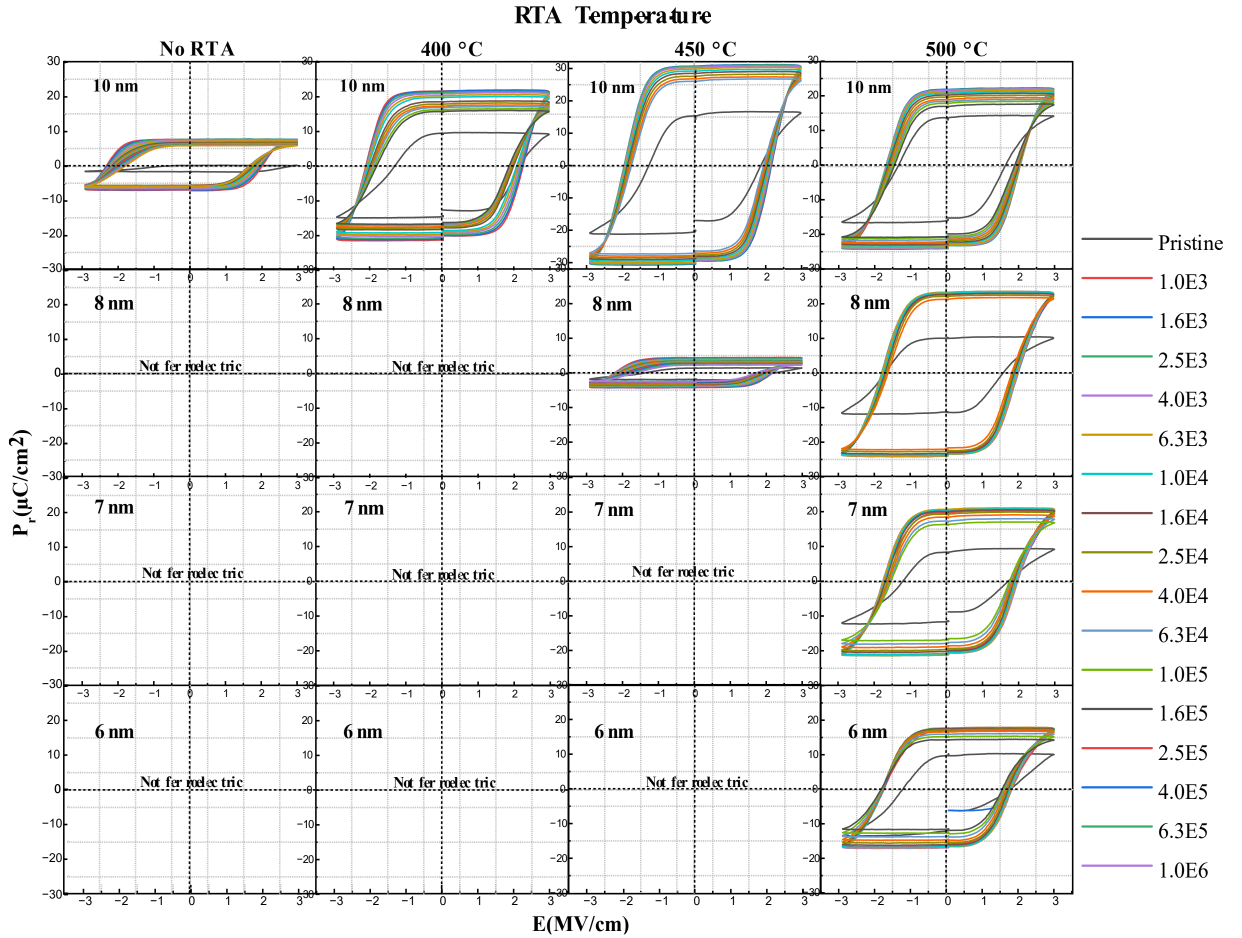

Figure 4.26: evolution of P–V hysteresis loops for samples with an aspect ratio of 500/300 during electrical cycling at a frequency of 1 kHz.

The endurance behavior displayed in Figure 4.23 ($2P_r$ cycles plots), which summarize the remanent polarization taken from the same set of loops at 1 kHz, is directly correlated with these patterns. The 10 nm HZO has the greatest initial $2P_r$ for AR $_{300/300}$ samples, with values exceeding 45 µC/cm². After around 10^4 cycles, there is a noticeable drop, indicating the start of fatigue. Despite having lower initial $2P_r$ values, samples with thicknesses of 8 nm and 7 nm exhibit more stable polarization over a larger cycling range. The ferroelectric phase is either missing or suppressed below a threshold thickness, as demonstrated by the 6 nm sample's negligible ferroelectric response.

The relationship between HZO thickness and endurance stability is highlighted by both the loop evolution and the derived $2P_r$ values. Significantly, the thickness-dependent

fatigue behavior of ferroelectric HZO films may be directly observed thanks to the 300/300 aspect ratio, which permits accurate assessment of intrinsic switching behavior with decreased parasitic capacitance.

Chapter Five: Discussion

In this study, the effects of three parameters: HZO film thickness, RTA temperature, and structure aspect ratio, on the ferroelectric performance of 3D HZO capacitors were systematically investigated. Through comprehensive structural GIXRD and electrical (PUND, endurance) characterizations, the study concluded that the aspect ratio plays a significant role in 3D architectures. This research successfully determined the optimal thicknesses and annealing conditions required for crystallization into the ferroelectric orthorhombic phase, and compared device performance across two distinct aspect ratio configurations.

5.1 Crystallization Threshold and Temperature Optimization

Based on the understanding that thin HZO films are more difficult to crystallize at relatively low RTA temperatures, the study postulates that increasing the annealing temperature enables crystallization to initiate within a specific transition temperature range. For instance, a 7 nm-thick HZO film may begin to crystallize at a certain threshold within that range, whereas a slightly thinner sample (e.g., 6.5 nm) may remain amorphous under the same conditions. Therefore, to ensure consistent and comparable ferroelectric behavior across all samples, a sufficiently high RTA temperature was deliberately selected; one that exceeds the transition range. This approach ensures that both aspect ratio groups undergo complete crystallization, allowing for valid structural and electrical comparisons.

The transition ranges for crystallization of HZO layers were found to be strongly thickness-dependent, with each thickness exhibiting a distinct minimum onset temperature for the emergence of the ferroelectric orthorhombic phase. Specifically:

- 10 nm-thick HZO films began crystallizing at 380 °C.
- 8 nm and 7 nm layers required at least 450 °C.
- 6 nm films required temperatures as high as 500 °C for observable crystallization.

These thresholds were consistent across both aspect ratio groups, indicating that thickness and thermal energy dominate the crystallization dynamics more significantly than geometric effects in this regime. From these findings, it can be concluded that:

- 10 nm-thick HZO layers exhibit ferroelectric behavior throughout the entire RTA temperature range tested (from 380 °C to 500 °C).
- All HZO samples, regardless of thickness or aspect ratio, exhibited robust ferroelectric response when annealed at 500 °C, confirming full crystallization into the orthorhombic phase at that condition.

This insight provided a consistent baseline for comparison across all experimental variables, ensuring that electrical and structural evaluations were conducted under crystallographically equivalent conditions.

5.2 Polarization Behavior and Aspect Ratio Influence

The ferroelectric behavior of the fabricated 3D HZO capacitors was evaluated through P-E measurements using the PUND technique. In agreement with the crystallographic insights from GIXRD, hysteresis loops were obtained for 10 nm-thick HZO samples annealed at multiple RTA temperatures, and All HZO thicknesses (6, 7, 8, and 10 nm) annealed at 500 °C.

These measurements were performed for both aspect ratio configurations: $AR_{500/300}$ and $AR_{300/300}$. The results revealed that, in general, the polarization window ($2P_r$) was consistently wider in samples with a higher aspect ratio (500/300). This enhancement can be attributed to increased effective electrode area in the 3D configuration, improved electric field concentration in high-aspect-ratio structures, and potentially more efficient domain alignment and switching dynamics.

However, an interesting exception was observed: For samples with lower HZO thickness (≤ 7 nm) and lower RTA temperatures (≤ 450 °C), the samples with lower aspect

ratio (300/300) occasionally exhibited a wider polarization window. This anomaly is likely due to:

- Incomplete or partial crystallization in thinner films under marginal thermal conditions.
- Better thermal uniformity or stress relaxation in shallower geometries during annealing, facilitating more effective phase transformation at sub-optimal temperatures.

These findings emphasize that aspect ratio becomes a dominant enhancement factor when ferroelectric phase formation is complete, while under marginal crystallization, simpler geometries may transiently outperform due to more favorable processing conditions.

5.3 Correlation between Crystallization and Polarization Performance

The observed deviations in polarization performance for some of the samples, particularly those annealed at RTA temperatures near the lower edge of the crystallization transition range, can be attributed to the sensitivity of phase formation to slight variations in film thickness. At these marginal temperatures, even minor deviations in nominal thickness (e.g., due to process variation or measurement error) may hinder the full development of the orthorhombic phase, resulting in incomplete crystallization and weak ferroelectric behavior. This explains why some samples, despite being close to the expected threshold, exhibited negligible remnant polarization ($2P_r \approx 0$).

These findings are consistent with GIXRD data, which indicated the absence of orthorhombic diffraction peaks in samples processed below their respective crystallization onset temperatures. This reinforces the idea that full ferroelectric behavior can only be expected once the annealing temperature surpasses a critical threshold that ensures complete phase transition, and that partial crystallization leads to suppressed or absent ferroelectric switching.

Furthermore, increasing the aspect ratio of the 3D capacitor geometry was shown to enhance the measured remnant polarization values, particularly when full crystallization was achieved. This enhancement is attributed to:

- The larger effective electrode surface area in high aspect ratio designs.
- Improved field uniformity and confinement.
- More extensive ferroelectric volume available for domain switching.

Thus, the remnant polarization in 3D HZO capacitors was observed to scale approximately proportionally with the surface area introduced by the 3D geometry, underscoring the significance of structural engineering in optimizing ferroelectric performance at nanoscale dimensions.

5.4 Comparison with Literature and Supporting Evidence

The experimental observations reported in this study are in strong agreement with previous findings in the literature on ferroelectric HfO_2 systems, including doped variants such as HZO. As reviewed by Ali *et al.* (2022), the minimum annealing temperature required to induce ferroelectricity in HfO_2-based films is influenced by both the choice of dopant (e.g., Si, Al, Zr) and the film thickness. For example, in Si-doped HfO_2 (Si:HfO_2), the orthorhombic phase was observed to emerge in 5 nm-thick films annealed at 700 °C, while equivalent films annealed at 600 °C remained non-ferroelectric.

A similar trend was reported by Hyuk *et al.* (2013), who studied HZO capacitors with varying thicknesses (5.5 nm, 10 nm, 17 nm, and 25 nm) across a broad temperature range (400–800 °C). Their results demonstrated that thicker HZO films crystallize into the orthorhombic phase at lower temperatures compared to thinner counterparts. These trends reinforce the central conclusion of the present study: the crystallization temperature threshold is both material- and thickness-dependent, and must be carefully tailored for reliable ferroelectric switching.

These literature benchmarks validate the experimental strategy adopted in this work, particularly the deliberate selection of high RTA temperatures (up to 500 °C) to ensure complete crystallization across all investigated thicknesses. They also support the broader implication that precise thermal and geometric control is essential in optimizing ferroelectric phase formation in advanced 3D capacitor architectures.

5.5 Supporting Findings from Literature on 3D Integration

Further validation of the findings in this study comes from the work of Grenouillet *et al.* (2023), who demonstrated that 3D-integrated HZO capacitors with 10 nm-thick HZO layers exhibit up to 1.3 x higher remnant polarization values compared to their planar (2D) counterparts. Although their work employed different annealing protocols and distinct electrical measurement techniques, the results are nonetheless complementary and affirm the central thesis of this study: increasing the effective 3D surface area proportionally enhances ferroelectric switching strength.

Importantly, the observed enhancement in $2P_r$ did not come at the expense of endurance, maintaining device reliability over extended cycling. This suggests that 3D integration offers a scalable path toward higher-density ferroelectric memory applications without degrading reliability. These external findings support the conclusion that structural design, particularly aspect ratio and surface architecture is a key lever for optimizing ferroelectric performance in next-generation non-volatile memory devices.

5.6 Conclusion

The findings of this study underscore the critical role of structural engineering and thermal processing in optimizing the ferroelectric performance of HZO-based 3D capacitors. Through systematic variation of HZO film thickness, RTA temperature, and 3D aspect ratio, it was shown that careful control over these parameters can lead to: Enhanced remanent polarization, Improved phase crystallinity, and Extended endurance performance.

In particular, increasing the effective 3D surface area proved to be a powerful design strategy, enabling stronger and more stable ferroelectric responses without compromising device reliability. These results align with recent literature and contribute to the expanding body of knowledge that supports 3D integration as a viable pathway for future ultra-dense, energy-efficient, and scalable non-volatile memory technologies.

This work not only advances fundamental understanding of HZO ferroelectricity in 3D architectures but also provides a solid experimental basis for continued exploration into next-generation ferroelectric memory devices. These insights pave the way for the rational design of future 3D ferroelectric systems with tunable and robust performance characteristics.

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تطوير وتوصيف مكثفات ثلاثية الأبعاد بعازل مرتكز على أكسيد الهافنيوم زركونيوم للذاكرة الفروكهربائية غير المتلاشية عالية الكثافة

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الملخص

في هذه الأطروحة، تمت دراسة السلوك الاستقطابي الكهربائي في المكثفات ثلاثية الأبعاد المصنوعة من أكسيد الهافنيوم زركونيوم. تم تصنيع مكثفات على رقائق سيليكون بقطر 300 مليمتر بسمك يتراوح من 6 نانومتر إلى 10 نانومتر، باستخدام تقنيتي الترسيب الذري الطبقي والترسيب الكيميائي بالبخار. جرى تحليل الخصائص الكهربائية والبنيوية لهذه المكثفات من خلال دراسة تأثير ثلاثة عوامل رئيسية، وهي: نسبة البُعد الهندسي، سمك طبقة أكسيد الهافنيوم زركونيوم ، ودرجة حرارة المعالجة الحرارية السريعة.

تم تحليل البنية البلورية باستخدام تقنية حيود الأشعة السينية بزوايا انزلاقية، حيث أظهرت النتائج أن زاوية السقوط المثلى للحصول على أنماط حيود واضحة تبلغ 7 درجات. وقد لوحظ أن درجة التبلور تتحسن، وأن شدة القمم البلورية تزداد بزيادة كل من درجة حرارة المعالجة وسمك أكسيد الهافنيوم زركونيوم. كما بينت النتائج أن العينات ذات النسبة البُعدية الأكبر أظهرت شدة قمم أعلى مقارنة بتلك ذات النسبة الأقل. وقد أظهرت التحاليل البنيوية تكوّن الطور البلوري المتعامد. وتم تحديد درجة الحرارة المثلى.

لدراسة الخصائص الكهربائية ، تم اعتماد تقنية النبضات المتعاقبة لقياس الاستقطاب المتبقي الناتج عن حلقات الاستجابة الفروكهربائية. وقد تم اعتماد تردد 10 كيلوهرتز بعد إجراء اختبارات عند ترددات مختلفة. سجلت العينات ذات النسبة البُعدية الأعلى قيماً أعلى من الاستقطاب المتبقي، الذي لوحظ أنه

يتحسن أيضا بزيادة السمك ودرجة حرارة المعالجة. كما أظهرت اختبارات قوة التحمل أن العينات ذات السمك الأقل والتي تمت معالجتها بدرجات حرارة معتدلة قدّمت استقرارًا كهربائيًا جيدا ، حيث تجاوز أداء بعضها 10^9 دورة تشغيل قبل حدوث الانهيار الكهربائي. هذه النتائج تسلط الضوء على أهمية التصميم البنيوي ثلاثي الأبعاد ودور النسبة البُعدية في تعزيز السلوك الاستقطابي الكهربائي، كما تؤكد الحاجة إلى ضبط دقيق لكل من المعالجة الحرارية وسمك أكسيد الهافنيوم زركونيوم من أجل تحقيق أداء ثابت وعالي الكفاءة للمكثفات الفروكهربائية.

الكلمات المفتاحية : الفروكهربائي، أفلام أكسيد الهافنيوم زركونيوم ، نسبة البُعد، تقنية النبضات المتعاقبة، الطور المتعامد.